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NAVAIR AVIONICS MASTER PLAN.(U)
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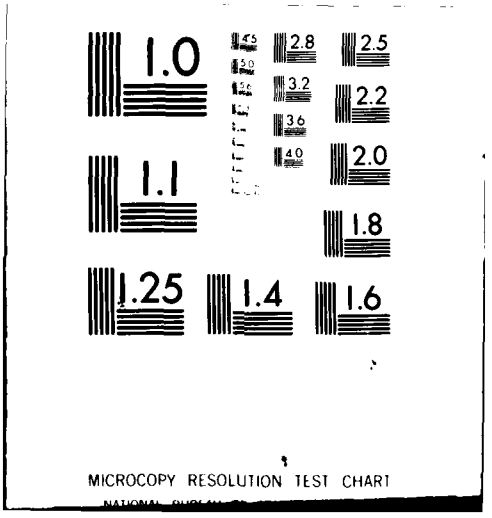
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NAVAIR AVIONICS MASTER PLAN.

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FOREWORD

This is the initial issue of the NAVAIR Avionics Master Plan (NAMP). It was prepared for the Naval Air Systems Command (NAVAIR), and is the product of inputs from NAVAIR, the Naval Air Development Center, Warminster, PA, and the Naval Avionics Center, Indianapolis, Indiana.

The purpose of the plan is to provide a comprehensive and authoritative working document to guide avionics developments, to focus resources and efforts on common avionics goals, and to assist in promulgating strategies and programs toward the resolution of problems and the meeting of avionics requirements.

It is recognized that this first issue does not provide total coverage of the broad spectrum of existing core avionics equipments, and does not provide concrete planning data for a direct tie-in to the Program Objectives Memorandum (POM) process. Also, it has not been possible to incorporate all comments provided on the November 1980 preliminary draft issue, primarily due to a lack of time. The NAMP is intended to be an evolutionary document; therefore, readers are encouraged to provide constructive comments, pertinent updating data, and suggestions for improvement so that subsequent issues will truly serve the Avionics community and will be in consonance with POM efforts. Comments/suggestions should be directed to the Naval Avionics Center, 6000 East 21st Street, Indianapolis, Indiana, 46218, Attention Code 074. (Autovon 724-3886, Commercial 317-353-3886)

It is planned that the NAMP will be updated and published annually, and that it will be expanded to cover Mission and Weapon Control Avionics in addition to the Core Avionics Topics now covered.

26 February 1981

Distribution: 1 copy except as noted ( )
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NAVAIR AVIONICS MASTER PLAN

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1. INTRODUCTION

1.1 NAVAIR AVIONICS MASTER PLAN (NAMP) DEVELOPMENT

1.1.1 OBJECTIVES

The objectives of the NAMP are to provide a comprehensive, authoritative document outlining a unified view of Naval avionics and to guide the decisions necessary to maintain and achieve required avionic equipment capabilities.

1.1.2 PURPOSE

The purpose of the NAVAIR Avionics Master Plan (NAMP) is to:

* Disseminate Naval Air Systems Command (NAVAIR) policy and guidance in all aspects of the development of Naval avionic equipment.
* Provide a single comprehensive document highlighting all aspects of Naval avionics - its current status, its requirements, and its long range objectives.
* Establish a planning baseline to serve as a foundation for overall advanced planning.
* Focus attention on management issues and technological problems that require resolution in the near term and on those special issues that require immediate attention to solve critical problems to ensure the orderly availability of needed avionic equipment.

1.1.3 SCOPE

The NAMP is a master planning strategy for the definition, assessment, and utilization of current and future Naval avionic equipment. The NAMP will cover all of the major facets of Naval avionics including requirements and objectives; readiness; reliability; maintainability; affordability; Integrated Logistic Support (ILS); Research, Development, Test and Evaluation (RDT&E); technology developments, opportunities, and obsolescence; and Conversion in Lieu of Procurement (CILOP) opportunities. The NAMP provides long range plans and alternatives for the achievement of a high level of avionic equipment capability projected over the next decade.

The NAMP is not intended to be a comprehensive listing of Navy avionic equipment or a substitute for, or duplication of, the Naval Avionic Equipment Installation Plan. The purpose of the NAMP is to identify current and projected developments and deficiencies and to establish prioritized courses of action to remedy those deficiencies.

This initial edition will deal only with core avionics. Subsequent editions will include both core and mission avionics. The NAMP is a new and evolutionary document. In the coming years, the contents will be expanded until all major issues related to long range planning and guidance are included.

1.1.4 STRATEGY USED IN PREPARING THE NAMP

In developing the NAMP, the following strategy was adopted:

* Improve the offensive capability of current weapon systems that depend on avionics through Research and Development and the procurement of new and improved avionic systems and components.
* Improve the effectiveness of logistic support structures.
* Exploit advanced technology to upgrade avionics equipment capabilities and reduce life cycle costs (LCC).
* Modernize the avionic components of current air warfare weaponry through the cost effective use of CILOPs.
* Identify ongoing and projected avionics developments.
* Strive to achieve higher levels of commonality, standardization, and multi-mission applications.
* Identify assumptions and alternative courses of action.
* Provide plans to achieve needed levels of readiness and sustainability in combat.
* Address costs of planned developments and improvements in relation to projected budgets and identify means of controlling LCC.

1.1.5 THE CHARACTER OF AVIONICS IN THE COMING DECADE

The character of avionics in the coming decade will be shaped and driven by several keystone technologies. The principal technology areas are:

* Fiber optics
* Integrated circuit technology, e.g., VHSIC
* Distributed data processing
* High speed signal processing
* High speed digital/analog conversion interface devices
* Semiconductor memory technology
* Display technology
* Microwave integrated circuits and dielectric waveguides
* Solid state microwave components
* Antenna technology

* Advanced self-test technology

* Microcircuit and modular packaging

* EO/IR/CCD/Laser technology

* Electro-acoustic device technology

* Computer (programmable element) technology

* High Order Programming Languages

The avionics of the 1990 era, which will embody these keystone technologies, must satisfy the changing requirements brought about by new vehicle developments and roles, changing threats, new weapons systems, and new operational concepts. The imperative need for minimum system size and weight, constraints on number and size of weapons/stores, criticality of take off and landing flight regimes, and potential for rapid lateral maneuvering all combine to create new challenges to the avionics designers. Likewise, the VSTOL concept, in order to become viable, demands new innovations to reduce cost, size, and weight and to achieve autonomous operations.

The coming decade will bring radically improved capabilities in the area of electronics and avionics, provided that we move forward in technology development in the meantime. Digital integrated circuit technology will continue to provide the primary basis for changes at all levels of avionics--both the on-board systems and support systems.

LSI and VHSIC technologies are key elements in effecting major changes in the complexion of avionics at all levels -- modules, Weapons Replaceable Assemblies (WRAs), subsystems, and systems. An obvious benefit of LSI and VHSIC is the reduction in size of circuitry, which takes place at the module level, but which is reflected up the line into smaller WRAs, subsystems, and systems. The big black boxes of the past will give way to smaller units. Besides helping to reduce overall system size and weight, it also permits more flexibility in the physical location of parts. This flexibility is a boon to the survivability and vulnerability designer, who can place the more critical items in protected places -- protected from hostile projectiles and from EMI/EMP.

Also, the advent of LSI microprocessors and microcomputers allows us to develop new architectures in our systems, resulting in integration and optimization of processing, extensive use of digital multiplex (MUX) buses, redundancy and separation of critical data handling facilities, a high degree of automation, fully integrated aircrew interfaces, significantly reduced dedicated avionics, and a high degree of hardware/software standardization.

A feature of the new architecture will be the extensive use of MUX buses which provide intra-system data communications over a few shared paths -- eliminating the need for large, heavy, and failure-prone avionics wire/cable harnesses.

For the near-term, these multiplex data paths will be either twisted shielded wire pairs or coax cables. This technology is sufficient to handle low data rates. However, it would be desirable to change the data paths to fiber-optics bundles to accomplish several desired results. First, it will be useful at very high data rates, sufficient to handle radio frequency information. It also diminishes the vulnerability of the data paths to extraneous interferences from EMI and EMP. The use of such standardized architecture, standard MUX buses, standardization in power sources and heat exchangers, and also standards in choice of computer languages pave the way for introducing "modularity" -- an old concept, but one which was not heretofore feasible. The natural consequence of modularity is "missionizing" -- namely customizing a system to do a particular job by adding/changing modules, thus allowing one basic airframe/vehicle to be used for any of several mission types without having to be "full-time" multi-mission.

The avionics revolution goes beyond missionizing and includes special impact in the sensors technology area. The sensor area will capitalize on solid state microwave components and circuits, synthetic aperture radar (SAR) concepts, Advanced Integrated Display System (AIDS)/Digital Avionics Information System (DAIS) display technology, lightweight and low cost conformal array antennas with electronic beam steering, modular radar packaging, and multiple sensor processing systems. The navigation area will benefit from the use of strapdown inertial platforms and the new, precise positioning systems such as Global Positioning System (GPS) and Joint Tactical Information Distribution System (JTIDS). Ring laser gyro inertial platforms will become operational in the mid 1980s. And, flight control systems will employ fly-by-wire techniques extensively.

At first glance, satellite communications and navigation aids hold great promise for the 1980's and 1990's. However, the military must not become totally dependent on them due to their vulnerability to attack. Alternate means of communicating and deriving navigation data must be included in systems design.

The benefits of "missionizing" carry over into the field of electronic warfare (EW), especially. A high degree of flexibility is required -- flexibility to rapidly react to changing threats. The needed flexibility will be afforded largely by reprogrammable EW subsystems and interchangeability of hardware units -- changing frequency coverage, offering modulation options, adapting automatic reaction logic, etc.

Flexibility to adapt to new weapons and weapons mixes will be designed in from the outset, providing sufficient data processing capability plus standard, general-purpose interfaces to handle new weapons designed according to well-documented interface standards.

The 1990 system will be unusable if Electromagnetic Interference (EMI)/Electromagnetic Pulse (EMP)/temperature/shock environments are not successfully combated. Adverse environments will be circumvented, or compensated for, using the technologies developed within those disciplines. Even the trends in aircraft construction, i.e., composite materials, tend to make

the avionics less protected and, hence, more vulnerable. New technologies destined to aid in this area of concern include: (a) use of lower power, yet high speed, semiconductor devices -- silicon-on-sapphire (SOS), gallium arsenide (GaAs), and eventually Josephson's devices; (b) use of fiber optics data paths; and (c) better placement/shielding/ redundancy of critical devices.

This forecast represents a radical departure from our historic avionics past. Such a drastic change will not be made without some reluctance and opposition. Even the changeover from analog to digital has been a gradual and agonizing change. It is predictable that architectural changes and standardization of avionics at subsystem and lower levels will be equally hard to effect. The process will be facilitated if the advanced technology concepts are incorporated in the system requirements and permeate downward in a "top-down" system design as opposed to the more familiar "bottom-up" approach.

The top-down design approach will offer another significant benefit, namely setting of requirements at the lowest level consistent with the mission, resulting in a less complex and consequently lower cost design. (This cost issue must be faced squarely, lest we bankrupt ourselves in buying more and more complex systems.)

The one area which is currently creating the greatest problem in avionics systems costs is not the high cost of elaborate hardware, but, rather, of software. Fortunately, the problem is not without a solution. Software science is in its infancy and needs to be brought along toward maturity. Growth of this science will be marked by the development of new structured approaches, better documentation, standardization of languages and procedures, increasing commonality of systems at the algorithm level, and improved software maintenance. The over-all result will not be inexpensive software, but it will be, hopefully, affordable and a more favorable percentage of total system cost on a LCC basis.

On a LCC basis, other major contributors to avionics cost, aside from initial hardware procurement costs, include maintenance and repair, operator training, and auxiliary equipment/spares. To attack these problems requires a conscious and organized effort on the part of all who are involved in a system design -- from the very outset. The concepts will best be addressed and engendered in a structured top-down avionic system synthesis, system integration, and system acquisition process where the system is designed and developed as a whole unit rather than as a loosely related set of components and subsystems.

2. AVIONICS OBJECTIVES

2.1 GENERAL

The purpose of this section is to identify a set of avionics objectives that will provide a management perspective to guide the identification, development, acquisition, and support processes required to field new avionic components and systems to meet projected requirements, and to foster the orderly upgrading of existing Fleet equipment through well planned and well executed modification programs. In structuring these objectives, reference has been made to guidance provided by the Naval Aviation Plan, CNO Objectives for 1980, Naval Air Systems Command Management Goals for Fiscal Year (FY) 1981, and AIR-05 Group Management Goals for FY 1981. Integrating this resource material, a set of objectives applicable specifically to avionics has been developed.

2.2 OBJECTIVES

These objectives have served as a guiding instrument for development of this NAVAIR Avionics Master Plan, and further serve as guidance for Acquisition Managers in the preparation of project plans for specific avionics projects. It is considered essential that avionics acquisition projects be structured around these objectives in order that avionics equipments provided to the fleet can maximize our combat capability and readiness in today's environment of limited manpower and funding resources.

2.2.1 DEVELOP INNOVATIVE, PRODUCIBLE, RELIABLE, MAINTAINABLE, AND SUPERIOR AIR WEAPONS SYSTEMS THAT MAXIMIZE COMBAT CAPABILITY AGAINST PROJECTED ENEMY THREATS.

This is an all-encompassing objective to which all other objectives could be established as a subset. While lacking in specificity, this objective serves as an overall reminder to Navy planners and implementers of the "bottom line" for all avionics acquisition actions.

2.2.2 IMPROVE FLEET READINESS.

The attainment and maintenance of a high level of Fleet readiness have been established as high priority goals for many years. This emphasis has been evidenced by the management support for formal reliability, maintainability, and logistic support programs for new avionics equipment developments. In-service readiness has been addressed through an aggressive Aircraft Equipment Reliability and Maintainability Improvement Program (AERMIP). AERMIP has demonstrated successfully that structured reliability and maintainability programs can yield an improved Fleet readiness posture. Continued emphasis on improved readiness for both new development and in-service equipment is required. This area is particularly challenging in the present environment in which our avionics equipment is characterized by increasingly complex system mechanization and expanding performance demands.

2.2.3 IMPROVE MANAGEMENT EFFECTIVENESS AND EFFICIENCY THROUGH SYSTEMATIC PROGRAM/PROJECT PLANNING AND CONTROL PROCESSES.

Inherent to the achievement of this objective is the establishment of an improved planning and budget process. The development of this NAVAIR Avionics Master Plan is a major step toward this objective. It is intended that the planning information within this document will serve as the basis for inputs to the Navy's five year Program Objectives Memorandum (POM). Improved planning must be a continuing effort encompassing a wide spectrum of operational, technical/technology, support and resource considerations, with overall guidance provided by Navy policy/ planning documents. Planning elements include, but are not limited to: optimizing trade-offs between new starts versus modification/CILOP (Conversion in lieu of Procurement) of existing assets versus use of existing NATO/ other service/commercial equipment; reconciling priorities with other planned developments and technology breakthroughs; assessing and minimizing risks; realistically evaluating funding and schedule constraints; structuring acquisition strategies to achieve competition during development as well as production; and identifying logistic support concepts and resources. Finally, effective and efficient planning requires open dialogue between the research and technology (AIR-03) function, maintenance engineering (AIR-04) function, and the systems and engineering (AIR-05) function.

2.2.4 CAPITALIZE ON ADVANCED TECHNOLOGY.

The potential advantages in the performance, weight, size, reliability, power dissipation, and life cycle costs of avionics that can be realized through the judicious application of advanced technologies have been quoted many times over. These "potential" advantages can become reality only if a commitment is made to invest the front-end funding resources required for implementation and control of advanced technology devices, forms, or processes. The necessity for such action has been well stated in the Naval Aviation Plan: We must maintain and, where possible, increase our qualitative edge in order to assure the necessary margin of naval superiority.

2.2.5 IMPROVE UTILIZATION OF TECHNOLOGY BASE PROGRAMS.

This objective relates to the need to improve the process for transfer of exploratory and advanced development technology into engineering development programs in a logical and efficient manner. Such improved utilization is dependent upon the Navy's ability to:

* incorporate effective and efficient technological forecasting and technical threat assessments in the systems alternative definition and selection processes,

* establish effective working interfaces and information transfer mechanisms with all relevant technology base administration and information centers, and

* maintain continuous technical opportunity and technical requirements exchanges between the research and technology function and the systems and engineering function.

The Assistant Secretary of the Navy (Research, Engineering, and Systems) and the Chief of Naval Material have established a plan to strengthen the coordination and management of Navy technology programs. The plan assigns the Chief of Naval Research with additional responsibilities as the Deputy Chief of Naval Material (Technology), and the Chief of Naval Development. These responsibilities will include the implementation of a revised management process for the planning and execution of the Navy's exploratory development programs. To support these functions, the Office of Naval Technology (ONT) has been established. These actions are expected to ease the problems of transitioning technologies into the advanced development stage.

2.2.6 INCREASE THE USE OF COMPETITIVE ACQUISITION.

The goal of any acquisition strategy should be to optimize the capability/quantity/supportability of weapon systems delivered to the Fleet through the least costly process available. The use of competitive acquisition techniques and multi-year procurements affords the opportunity to realize lower acquisition costs while at the same time enhancing production capability for production rate increases or mobilization requirements. In essence, competition or at least the threat of competition provides a hedge against the uncontrolled cost growth and the poor schedule performance frequently encountered in sole source situations. Competitive acquisition during both the development and production phases should be pursued vigorously.

2.2.7 BRING ACQUISITION PROGRAMS IN ON-TIME AND ON-COST.

The completion of on-going acquisition programs within allocated schedules and budgeted funds must be a continuing management goal. A strong technical corporate memory, based on technical and production specialists with "hands-on hardware" expertise, provides a means for dealing with contractors from a position of knowledge and strength. Increased utilization of field activity and laboratory support should continue to be pursued to enhance NAVAIR Headquarters program and technical management support.

2.2.8 APPLY COMPREHENSIVE AND CREDIBLE COST ANALYSIS TECHNIQUES.

Comprehensive and credible cost estimates are as much a part of planning and selling an avionics new start program as they are in controlling cost levels within on-going programs. Computerized cost estimating techniques have matured to the extent that they are now a viable approach for comprehensive, credible, and professional cost estimation and prediction. Computerized cost estimating techniques and the processes/procedures for their application to acquisition projects/programs must be exploited.

2.2.9 REQUIRE ALL PROJECTS/PROGRAMS TO BE SUBJECTED TO RIGOROUS STANDARDS OF RELIABILITY AND MAINTAINABILITY.

The NAVAIR "New Look" Program has reaped benefits in terms of improving the reliability and maintainability of recently fielded avionics equipments. The momentum of this initiative must be increased, since Fleet readiness and cost of ownership are related directly to these equipment characteristics.

3. FORCE MODERNIZATION

There are a number of efforts underway to effect overall Naval Aviation force modernization. This section will deal primarily with the approaches to upgrade avionic equipment utilizing modern mature technology. The Aircraft Equipment Reliability and Maintainability Improvement Program (AERMIP) is aimed at improving reliability and maintainability (R&M) of existing avionics by the judicious use of new technology in a cost effective manner. The Conversion in Lieu of Procurement (CILOP) efforts, however, emphasize improving system capabilities to meet new threats/ requirements as well as improve R&M. CILOPs are being performed on various platforms (e.g., ships, aircraft, and weapons) in an effort to extend the useful life of the equipment in the Fleet as a cost effective alternative to new procurements.

Careful planning and analyses are required in both of these modernization efforts to ensure that equipment upgrades are applied in appropriate situations and that only mature and reliable technologies are utilized. With the advent of mature processor technology and the acceptance of data bus techniques, CILOPs can now utilize data bus architectures which are much more flexible and tightly integrated. Future system modifications can be made with software/firmware as opposed to significant hardware impacts/changes. Also, because of the interaction between the various subsystems, it will be essential to evaluate total system performance in a hot bench mock-up after subsystem(s) have been modified. Given that the data bus interfaces are well defined and properly utilized, there exists the potential to standardize on subsystems and to provide subsystems as Government Furnished Equipment (GFE) for multiple platforms which will result in significant life cycle cost savings.

Technology developments must continue to be emphasized to assure the continued success of providing equipment which meet changing threats. This is true for new aircraft as well as aircraft upgraded by CILOP/SLEP/AERMIP efforts.

A significant increase in the number of CILOP/SLEP efforts will result in a funding requirements shift from new aircraft procurements to aircraft rework funding. The AERMIP efforts need to show cost effectiveness before they are undertaken, but the cost avoidance is usually maintenance and spare parts related.

These efforts represent significant steps toward integrating new technologies into Fleet equipment in the most cost effective ways in order to make maximum utilization of the current assets. The other approach to Fleet modernization, of course, is to procure new aircraft to meet anticipated threats. New aircraft procurement plans are not covered in this section.

3.1 CONVERSION IN LIEU OF PROCUREMENT (CILOP) EFFORTS

3.1.1 Background

A rapidly changing threat environment, coupled with ever increasing development costs and decreasing or constant budgets, result in a decreased ability to field new airborne platforms. In order to meet the essential need of an adequate number of capable aircraft within the budget, various platforms

are undergoing or are being considered for a Conversion in Lieu of Procurement (CILOP) and/or a Service Life Extension Program (SLEP) effort. A SLEP results in the restoration or replacement of the airborne platform primary structure and/or the engines and drive trains which have reached a fatigue or age limit. A CILOP effort is most often accompanied or proceeded by a SLEP, and emphasizes the upgrading of the avionic equipment to meet the perceived threats and increase system reliability/ maintainability (R/M). An extensive analysis must be conducted for each platform to evaluate whether it is more cost effective to perform CILOP/SLEP efforts or to procure new equipment.

Many factors need to be considered in this type of an analysis, such as current age of the platforms, performance capabilities of the airframe and avionics, threat analysis including allocation of threats to be countered by this development/modification, capabilities of new technologies, life cycle costs, and potential multimission role or a new role for a specific platform.

3.1.2 Current Status

The Sea Based Air Master Study CILOP/SLEP Task report of 15 December 1979 summarized extensive investigations into the alternative approaches to Fleet modernization utilizing the CILOP/SLEP upgrade programs. Several "most logical candidates" were examined in this investigation including A-6E, KA-6D, A-7E, F-14A, E-2C, S-3A, SH-2F, SH-3H, and CH-46E. This task addressed only what could be done with existing aircraft and did not analyze force level requirements. The designs and estimated costs were provided by the original aircraft contractors for (1) a SLEP only, (2) a SLEP plus an austere system upgrade to "minimally" meet the threats, and (3) a SLEP plus a full capability upgrade to "fully" meet the threats postulated for 1990, 1995, and 2000. The austere systems were not to consider a complete redesign of the system configuration, but the study concluded that several aircraft types could not meet the threats without a complete redesign. Other significant results include the following:

* The advanced age of some of the aircraft indicate that extensive rework is necessary.

* Pacing technologies are very significant drivers in the success of many aircraft modification designs.

* NATO interoperability was lacking in all designs.

* Consideration of survivability enhancements was limited.

* Both new aircraft and CILOP upgrades require the continued development of new technologies to meet an improving threat. CILOP is no substitute for technology development.

* If a significant number of CILOPs are initiated, there would be a funding requirements shift from new aircraft procurements to rework efforts, and additional RDT&E funding would be required for this rework for initial design development.

* The cost estimates for the CILOP redesign efforts were considered to be very high.

Currently, some CILOPs are in process and others are being investigated.

3.1.3 Perceived Trends

The CILOP redesigns were proposed by the original contractors involved in the production of each aircraft. As a result, the designs do not in general reflect an adequate degree of standardization in the choices of avionics architecture, subsystems, components, or data buses. Some common Government Furnished Equipment (GFE) equipments such as the AN/AYK-14(V) Standard Airborne Computer are not being consistently utilized in the redesigns, and different variations are appearing in the implementation approach to the MIL-STD-1553 multiplex data bus.

Since the cost of a one-step major system redesign of a CILOP effort is significant, some acquisition managers are evaluating the use and cost effectivity of a number of more moderate, time-phased modifications to the existing subsystems to meet the threats. This has the effect of perpetuating a large number of non-standard subsystems. Unless a data bus architecture is introduced in an early phase, future integration efforts are more difficult, and system flexibility and growth are hindered. Modifying old equipment also worsens an already severe problem which is the obsolescence of high technology semiconductor devices used in the equipment and the lack of Navy knowledge of what technologies (device types) are used in each subsystem. This problem is being addressed by the NAVAIR COMPRESS/IMPACT Program, but additional efforts are needed.

With the advent of avionics that employ distributed processing, data buses and reconfigurability, there is much more interaction between the subsystems. This precludes the stand-alone testing of individual subsystems and mandates evaluation of the subsystem performance in an all-up system (or system simulation). More system "hot-benches" or integrated test facilities (ITFs) are being utilized to test, evaluate modifications, and maintain configuration control. Avionics systems that previously did not require an ITF, may find the need for one.

As stated earlier, the CILOP redesigns that have been evaluated have been deficient in NATO interoperability and in survivability enhancements. These trends need to be reversed.

3.1.4 Areas Requiring Further Development

Current - Analyses of the cost effectivity of a CILOP approach need to be continued for aircraft that are projected to be unable to meet anticipated threats. The Sea Based Air Master Study CILOP/SLEP Task investigation identified several aircraft which would need to initiate a CILOP effort in the near future.

Short Term (0 to 5 years) -

* Guideline documentation is required for use by contractors proposing CILOP avionics upgrades to ensure maximum use of standardization, data bus architecture, and appropriate use of new technologies.

* The COMPRESS/IMPACT Program needs to be implemented and applied to CILOP contracts.

* The MIL-STD-1553B multiplex data bus needs further definition because several of the designer-defined options can result in incompatibilities. A specification is being prepared by NAVAIR to accomplish this definition and should be imposed on all CILOP applications in which a dual redundant, serial, time division multiplex bus will suffice.

* Additional funding will be required in the aircraft modification (including RDT&E) budget to accommodate anticipated CILOP efforts.

* Continued emphasis must be placed on funding carefully selected new technology developments which could increase the capabilities of new or upgraded systems.

Mid Term (5 to 10 years) -

* Investigation of advanced avionics architecture and data buses should continue and the resulting recommendations made available to acquisition managers and contractors. Emphasis should be placed on systems which are reconfigurable and possess the capability to degrade gracefully without catastrophic failure to critical functions when subsystem failures occur. Continued development of interface standards (electrical, mechanical, and thermal) is needed.

* Techniques need to be developed to effectively use ITF installations to evaluate subsystem performance, and to maintain configuration control (hardware, software and firmware).

* Guidelines and NATO interoperability requirements need to be developed and invoked to ensure growth in the effectiveness of the NATO forces.

Long Term (10 years plus) -

* Since the trend is toward longer aircraft service life, investigations should be made into aircraft/avionics system implementations that will facilitate easier (and less costly) CILOP modifications. Examples are avionics that are functionally partitioned with well defined interfaces that can be easily removed and replaced with a new subsystem, utilizing modern technology, that performs an enhanced version of the same function.

3.1.5 Development Priorities

* MIL-STD-1553B specification approval and implementation.
* Continued analysis of high potential CILOP candidate aircraft.
* Preparation of CILOP avionics upgrade guidelines for maximum use of standardization.
* COMPRESS/IMPACT Program implementation.
* Continued new technology developments.
* Develop and implement ITF utilization techniques.

3.1.6 Summary

The CILOP/SLEP approach to force modernization can be a cost-effective and timely technique to maintain a needed force level and meet improved threats. Care must be exercised to perform an accurate cost trade-off and to ensure that contractors make maximum utilization of standardization and appropriate utilization of new technology.

3.2 AIRCRAFT EQUIPMENT RELIABILITY AND MAINTAINABILITY IMPROVEMENT PROGRAM (AERMIP)

3.2.1 BACKGROUND

In recent years, the increased complexity of avionics systems on tactical aircraft has been accompanied by system readiness degradation. Due to this continuing system degradation, a serious shortfall in aircraft readiness index is currently being experienced by the Naval Air Forces. Factors responsible for the system degradation include functional areas such as avionic system/equipment design and procurement policies, weapons system age, existing maintenance facilities and procedures, and the tactical aviation mission environment.

Through Fleet experience on deployed equipments, aircraft maintenance reporting, and contractor participation, the Reliability and Maintainability (R&M) aspects of aviation systems have been identified as two prominent elements of the readiness problem. Studies and investigations conducted for the Chief of Naval Operations have shown that one of the most serious deterrents to achievement of the hoped for operational efficiency in Navy task forces is the low Mean Flight Hours Between Failures (MFHBF) record of a great many of the in-service systems and equipment, particularly those classified as avionic.

R&M deficiencies stem from the classical causes, i.e., those related to equipment design, eventual breakdown of component characteristics, degradation of vendor production procedures, or system operation under extreme environmental conditions. Most recently, system maintainability is being jeopardized because many of the microcircuit devices with which yesterday's avionics are constructed will become obsolete, and hence unavailable to support future requirements.

The Aircraft Equipment Reliability and Maintainability Improvement Program (AERMIP) is a significant and continuing effort for R&M improvement of in-service equipment to meet the need for measured increases in tactical aircraft material readiness. The program is structured such that before work commences on an AERMIP project, there must be a commitment by the Equipment Manager to obtain production and retrofit funding for the improved equipment. AERMIP provides funding for the nonrecurring engineering efforts required to upgrade in-service aircraft equipment found to be deficient in R&M characteristics. However, tasks to improve specified equipment performance (increased range, sensitivity, accuracy, speed, altitude, etc.), ground support equipment, or air-launched weapons are excluded from consideration.

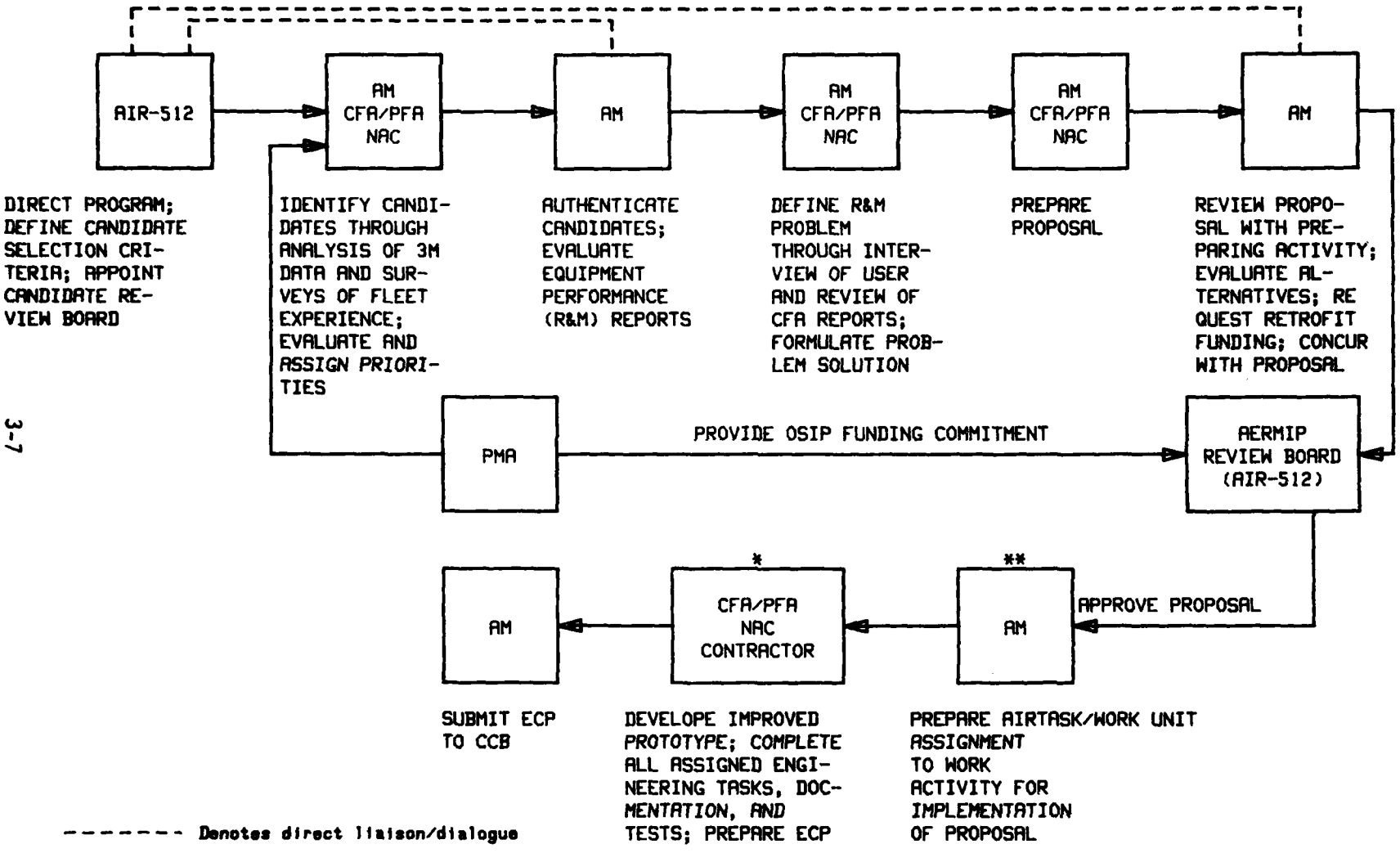
3.2.2 CURRENT STATUS

AERMIP's charter currently includes equipments used on land-based tactical aircraft in addition to carrier-based aircraft. Typical AERMIP candidate equipments generally contain out-dated technology electromechanical modules, vacuum tube circuitry, or early solid state technology components which exhibit high failure rates or are becoming increasingly difficult to procure. These systems are usually high cost, large quantity items whose complete replacement with operationally equivalent, new production, state-of-the-art equipment is economically impossible. For AERMIP consideration, the equipment problems must be such that through AERMIP, significant improvement to R&M can be achieved. The current standard used to determine if the improvements are significant is a projected payback period of 3 years or less. AERMIP is divided administratively into two areas. The first area is responsible for the candidate identification, prioritization, justification, and improvement proposal submittal. The second area is responsible for the management of AERMIP equipment improvement projects which have been approved and funded. The AERMIP responsibility and processing flow is depicted in Figure 3-1.

The AERMIP candidate identification and justification personnel perform exhaustive research within all available maintenance and utilization data sources such as:

* Naval Aviation Logistics Data Analysis (NALDA) System
* Navy Maintenance Support Office (NAMSO)
* NAVAIR Engineering Support Office (NESO)
* Aviation Maintenance Engineering Analysis System (AMEN)
* Depot repair liaison
* Direct Fleet liaison
* Contractor data

AERMIP RESPONSIBILITY AND PROCESSING FLOW



-------- Denotes direct liaison/dialogue

*Involves an official contract through Field Activity if contractor is involved)
**Prepare work unit assignment where Field Activity involved
CFA (Cognizant Field Activity)
PFA (Participating Field Activity)
OSIP (Operational Safety and Improvement Program)
AM (Acquisition Manager)

FIGURE 3-1

A major area of importance considered during AERMIP candidate identification is the appropriate prioritization of prospective candidates. This process is designed to yield a listing of those equipments having the most deleterious effect on tactical aircraft, and therefore requiring attention first. AERMIP produces a ranking report that utilizes a composite ranking factor based on ten criteria which quantify the major components of degradation. These degradation components are as follows:

* Readiness

* Reliability

* Maintainability

Two versions of the listing are created. The first ranks equipment within a platform line. The second ranks common equipment across platform lines.

The funded project management area of AERMIP entails maintaining overall cognizance of each funded project by the NAVAIRHQ AERMIP manager.

To accomplish these ends when a contractor is involved, the NAVAIR cognizant engineer is responsible to the AERMIP manager for the following:

* Monitor Individual Project Funding

* Ensure Scope/Method of Improvement is Followed

* Request Deviations/Extensions When Justified

* Attain Milestones On Time and Within Budget

* Provide a Single Point-of-Contact for Liason Between NAVAIRHQ AERMIP manager and NAVAIR Field Activity/Contractor Engineers

When a NAVAIR Field Activity is involved in the AERMIP project, a Field Activity cognizant engineer is responsible to the AERMIP manager through the NAVAIR cognizant engineer for the above functions.

The depth of redesign is gauged solely on the improvement required to bring the equipment to an acceptable level of R&M.

* An example of an AERMIP project requiring minimal redesign is the CV-2428/ASW Data Link Digital-to-Analog Converter used on the F-4J/N. The effort was limited to redesign of a gated-comparator IC which was no longer commercially available and was impacting maintainability to the equipment.

* An example of an AERMIP project requiring extensive effort is the redesign of the AN/ALQ-99 Tactical Jamming Pod used on the EA6B aircraft. This effort includes corrosion preventive measures, turbo generator transient suppressant, redesign of Band 7 transmitter, and incorporation of a multi-band exciter.

3.2.3 PERCEIVED TRENDS

The capability provided by this program is becoming of increasing importance to aircraft efficiency and operational readiness as phase-out of aging equipment slows during the out-years. Because of shrinking defense budgets, an effective improvement program for existent avionics systems is seen as an economical alternative to wholesale proliferation of new equipments and materials that are subject to unknown failure modes and the resultant deleterious effects.

Of high priority for improvement will be candidates in the following categories:

* Discardable items that could be converted to reparables or be improved in reliability characteristics.

* Items or components in older equipment versions which can be replaced with recently developed components used in modern equipments of similar function.

* Items containing obsolete electronic components (or those approaching obsolescence) which will require replacement with improved components such as modern technology integrated circuits, microcircuits, and hybrids.

* Selective redesign of system elements, when the redesign of individual circuit elements or small assemblies cannot be shown to be cost effective.

As AERMIP has expanded since its inception, the interfaces with other established DOD readiness improvement programs have been and will continue to be refined for maximum improvement. Coordination relationships will increase with programs such as the following:

* Predict and Relook (PAR)

* NAVAIR Reliability Team

* Engineering Investigation Program (EIP)

* Analytical Maintenance Program (AMP)

* NAVAIR Field Service Representatives (NFSR)

* NAVAIR Engineering Service Unit (NAESU)

* Readiness Improvement Status Evaluation (RISE)

* Productivity, Reliability, Availability, and Maintainability (PRAM)

3.2.4 AREAS REQUIRING FURTHER DEVELOPMENT

3.2.4.1 Current Plans - In recognition of the need to prioritize equipments having equal levels of R&M degradation, the final developmental stages of implementing readiness degradation criteria into the AERMIP ranking report is in process. When two or more equipments have similar levels of R&M degradation, the addition of the readiness criteria will enable the Navy to concentrate on those equipments having the greatest impact on aircraft readiness. The inclusion of these criteria into one overall ranking will preclude the subjective resolution of differing ranks for the same equipment obtained from the NAMSO equipment degradation ranking report and reliability and maintainability summary report.

3.2.4.2 Short Term (0 to 5 years) Plan - In response to a request to apply AERMIP ranking procedures to other areas of NAVAIR interest, AERMIP is developing a presort technique so that a ranking can be created applicable to a specific area, i.e.,

* Core Avionics
* Mission Avionics
* Equipments applicable to specific Cognizant Field Activities

AERMIP will develop life cycle economic techniques to yield comparative redesign figures applicable to the following approaches.

* Piece part redesign vs SRA redesign vs total system redesign
* Circuitry redesign vs custom ICs/hybrids
* Circuitry redesign vs life-time buys of components approaching obsolescence
* Traditional redesign vs MAP/SEM redesign

3.2.4.3 Mid to Far Term (5 to 10 years plus) Plan -

* To continue AERMIP as a dynamic program, assimilating new technologies which provide equipment improvement without the need for total system replacement.
* To remain watchful for failure modes heretofore unseen such as:
  * Reversion of sealants, adhesives, and potting compounds
  * Delamination of composite materials as their aviation use expands
  * Breakdown of wiring insulation and connector dielectric in new, more exotic, materials.

3.2.5 SUMMARY

The significant R&M deficiencies found in the Navy's tactical aircraft on-board systems have a serious detrimental effect on aircraft readiness. For this reason, a vigorous and effective "get well" engineering program was required to substantially improve the R&M characteristics of in-service equipment. To accomplish this, AERMIP was established to incorporate modern and more reliable technology into prototypes of improved versions of equipment to replace those found to have detrimental R&M characteristics.

4. AVIONICS TECHNOLOGY/TRENDS

With the advent of numerous, promising new electronic technologies, design tools, and techniques, the Naval Air Systems Command (NAVAIR) has initiated programs to restructure design, development, material acquisition, and support operations to utilize management and control concepts that are equally as innovative and effective as the advanced electronic technologies that they will utilize and control. The following sections provide a description of intended actions in the areas of keystone technologies, technology application and obsolescence, software, and a description of architectural trends.

4.1 KEYSTONE TECHNOLOGIES

While many advanced technologies inherently possess the potential for reducing the cost of ownership and increasing the performance and reliability of avionics, their usage has been limited because of the necessary system development and technology development actions, with increased front-end development costs, required to implement them. If, however, total avionics costs are evaluated on a life cycle basis, use of advanced technology devices can prove to be cost effective in many applications. Avionics acquisition managers must be willing to invest front-end development costs, if the Navy is to achieve the cost savings that are possible with the optimum application of advanced technologies.

The following sections are included to provide a description of a number of these keystone technologies.

4.1.1 MICROWAVE DEVICES AND MICROWAVE INTEGRATED CIRCUITS

4.1.1.1 Background

Microwave devices and circuits are of increasing importance to military communications, electronic warfare and electronic countermeasures equipments. The increased application of microwave devices (those operating at frequencies above 1 GHz) is a direct result of technological advancements driven by over utilization of the lower frequency spectrum (resulting in signal interference) as well as adaptation to the changing threat environment.

Microwave components are primarily used in receiver front ends and transmitter output circuits. A Microwave Integrated Circuit (MIC) is a combination of active and passive elements manufactured on a single semiconductor substrate (monolithic MIC) or discrete devices integrated via transmission line techniques on an insulating substrate such as teflon, glass or ceramic (hybrid MIC).

In recent years, three main trends have prompted the growth of microwave devices and technology. The trends are:

* The increased power available in bipolar and field effect transistors,

* Increased demands by DOD for higher reliability and maintainability (R&M) as well as reduced acquisition costs, and

* New weight reduction requirements, due to increasing the avionics hardware requirements for already fully loaded airframes.

MICs offer a 3-to-10 times reduction in size and weight compared to earlier forms of planar and coaxial microwave circuit construction techniques. Maximum utilization of MIC technology will be influenced by advancements in the following areas:

* Semiconductor device developments,

* Complex integrated assemblies,

* Fabrication and packaging techniques, and

* Reliability and testing.

4.1.1.2 Current Status

A great deal of development and technological progress has been made in the microwave solid-state area. From a device viewpoint, there are five basic solid-state approaches to the generation and/or amplification of microwave power. They are transistors, Gunn diodes, IMPact Avalanche Transit Time (IMPATT) diodes, TRApped Plasma Avalanche Triggered Transit (TRAPATT) diodes, and Varactor Multiplier diodes. The greatest improvements are anticipated in the areas of transistors [both bipolar and field effect transistors (FET)], TRAPATT and IMPATT devices.

The silicon bipolar power transistor presently dominates circuit applications at frequencies up to 4 GHz with impressive efficiency levels. Figure 4-1 depicts current performance levels in all three classes of operation.

A very significant feature of the power transistor advancement has been package design improvements as well as device refinements. These include the development of Beryllia packages for better heat transfer and improved processes for higher device efficiency.

Power Gallium Arsenide Field-Effect Transistors (GaAs FETs) are coming of age. The low distortion, predictable gain, ultra-wideband capability, and high device efficiency of GaAs FETs have made this transistor group good candidates for the replacement of high frequency bipolar transistors, high-power Gunn devices and low-power IMPATTs. Due to the low noise figure and good third order intermodulation characteristics of GaAs FETs, this device also makes an excellent pre-amplifier for RF front end applications. Figure 4-2 is representative of current state-of-the-art technology of high power GaAs FETs.

CURRENT STATE-OF-THE-ART SILICON BIPOLAR TRANSISTORS

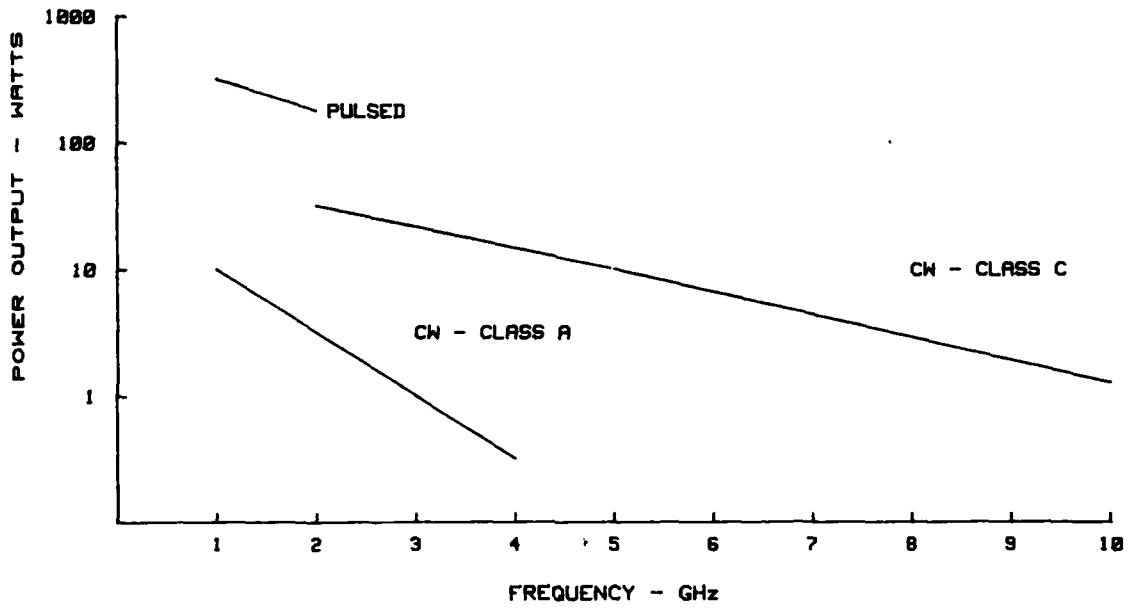


Figure 4-1

CURRENT STATE-OF-THE-ART
GALLIUM ARSENIDE FIELD-EFFECT TRANSISTORS

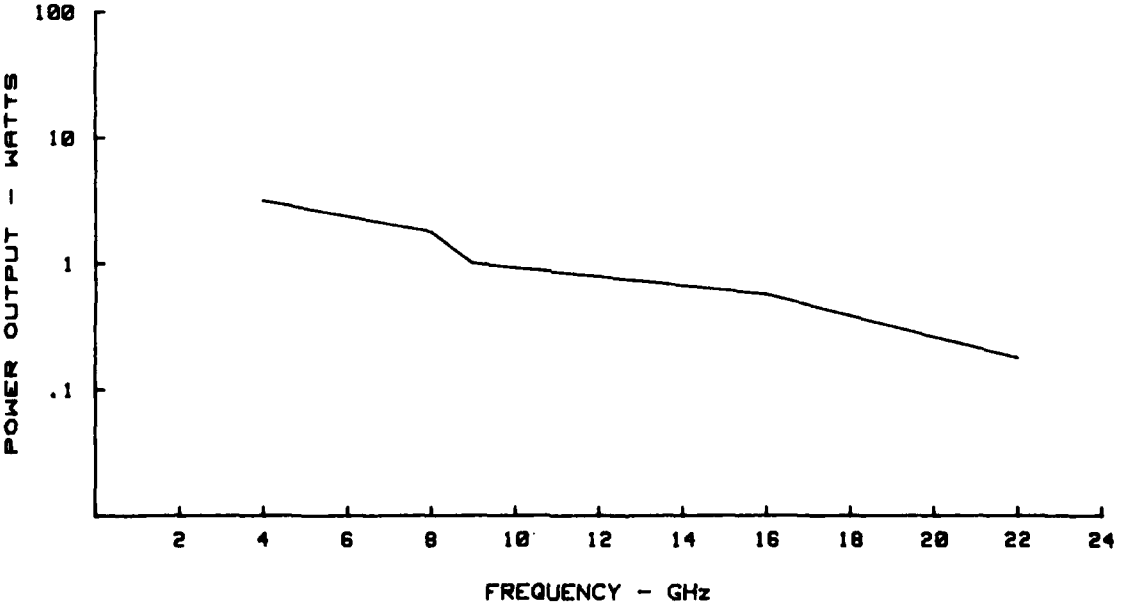


Figure 4-2

TRAPATT devices are two-terminal avalanche devices possibly suitable for certain applications in Electronic Countermeasures (ECM) and Electronic Counter-Countermeasures (ECCM) subsystems as power sources and amplifiers. The following problem areas must be addressed successfully for TRAPATTs to be considered. They include:

* Premature device failure under wide pulse width conditions due to mesa-surface degradation,
* Trade-off between power output and efficiency versus band width, and
* Reduction in noise output due to spurious oscillations.

Figure 4-3 illustrates current TRAPATT performance.

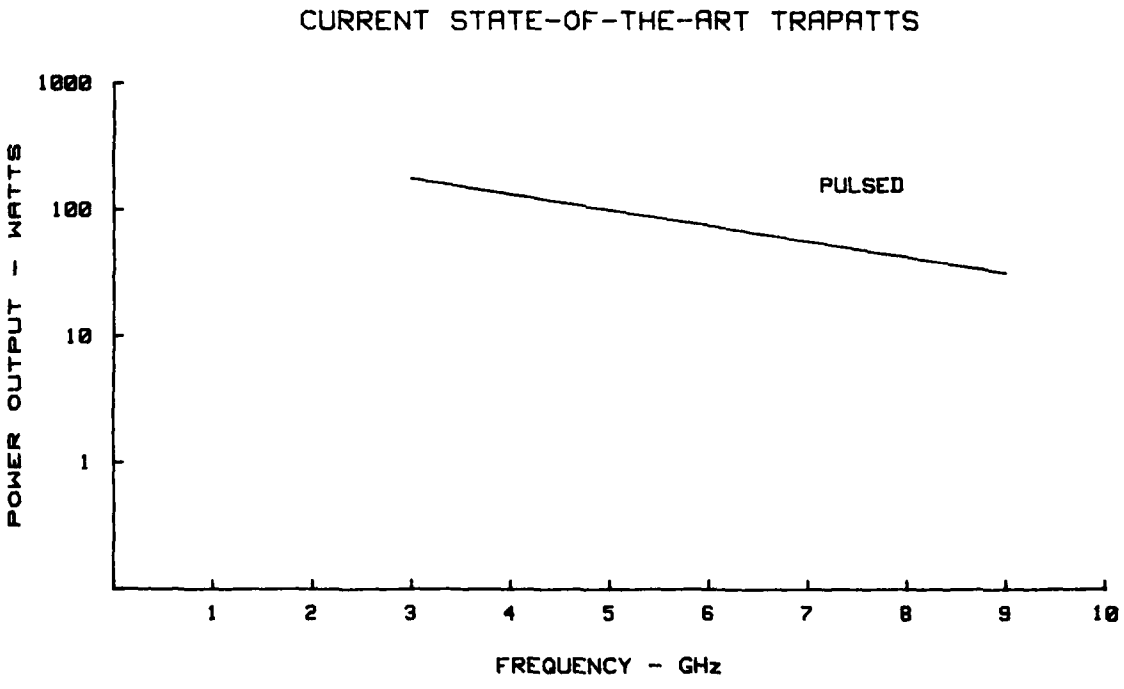


Figure 4-3

IMPATT devices are junction avalanche devices fabricated from either silicon or GaAs. They make use of either p-n junction or metal semiconductor (Schottky Barrier) junctions with drift regions on one or both sides of the junction. Potential applications include ECM and ECCM subsystems. Figure 4-4 is a presentation of the current state-of-the-art for both silicon and GaAs IMPATTs.

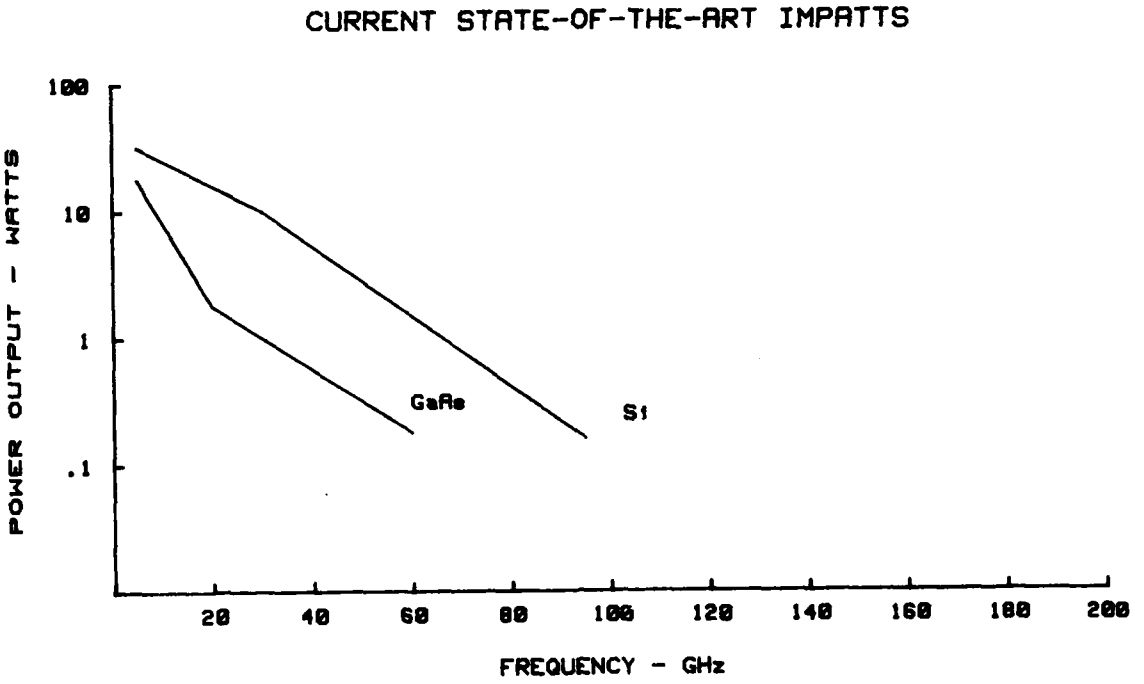


Figure 4-4

4.1.1.3 Perceived Trends

Solid state devices are being developed for higher power, greater efficiency and higher frequency of operation. The most rapid improvements are occurring in GaAs FET devices. Recently, the development of GaAs Monolithic Integrated Circuits has begun. This technology offers the opportunity of integrating microwave, analog and digital circuits together on the chip. The emergence of this technology can readily lead to a revolution in high speed signal processing.

In the 2-1300 MHz range FET technology has demonstrated good ruggedness, lower noise, and negative temperature coefficient. Power amplifiers will benefit from the use of this technology. Vertical Metal Oxide Semiconductor (VMOS) and Static Induction Transistors (SIT) devices in particular should be investigated for use in the above frequency range.

The approach of treating a complex network such as a receiver front-end assembly as a single "super component" is an emerging philosophy. The concept of performing a subsystem task within a single component package, using transmission line techniques, is the philosophy of Complex Integrated Assemblies (CIA). The concept involves more than the cascading of components within a single assembly. Specifically, it involves the definition of assembly input/output transfer functions, and the determination of those functions that can be synthesized and/or combined to minimize the number of component parts in an assembly.

The utilization of complex integrated assemblies can result in:

* reduction in network insertion loss,

* improved system amplitude and phase tracking capabilities,

* reduction in component parts,

* reduction in physical size of assembly,

* reduction in cost, and

* significant reliability increases.

Device fabrication and packaging techniques are advancing in the following areas:

* Use of electron beam lithography will result in higher frequency devices with sub-micron geometry.

* Improved methods of heat transfer using plated heat sinks, beryllia packages and refractory metal-gold metallization techniques allow higher power operation without a decrease in device reliability.

* New substrate materials such as porcelain, improved thick film conductor techniques, and better conductive bonding materials promise a reduction in assembly costs of MICs.

4.1.1.4 Areas Requiring Further Development

Current -

* Develop more repeatable active devices such as silicon and GaAs transistors. Only if these devices are repeatable from production lot to lot will the cost advantage of "no tuning required" MICs emerge.

* Develop standard hermetically sealed MIC packages including RF connectors. Currently, MICs are not hermetically sealed, and this is expected to lead to reliability problems, especially in at-sea environments.

Short Term (0 to 5 years) -

* Develop burn-out proof solid state power amplifiers to eliminate reliability problems caused by aircraft cabling and antenna mismatch.

* Develop solid state replacements for traveling wave tubes.

* Develop multiple sources for critical microwave devices and circuits.

* Implement better built-in-test capability in MICs.

* Develop improved methods for measurement of large signal parameters of microwave power devices.

* Develop a standard Computer Aided Design (CAD) program for use throughout DOD to improve standardization and technical interchange.

Mid Term (5 to 10 years) -

* Develop monolithic MICs to integrate RF, analog, high speed digital, surface acoustic wave (SAW) and optical technologies to achieve a true breakthrough in signal processing capability.

* Improve standardization of devices and circuits. A good candidate is the development of a programmable receiver front end.

* Continue to improve performance of microwave components for higher power and higher frequency applications.

Long Term (10 years plus) -

* Continue to develop monolithic MICs especially for use in missiles, drones, and lightweight platforms.

* Increase efforts to standardize on microwave devices and circuits.

4.1.1.5 Development Priorities

* Develop a family of standard hermetically sealed packages for MICs.

* Develop dielectric coatings as an alternate method of sealing MICs.

* Develop failure resistant solid state high power microwave transistors to replace high voltage vacuum devices such as traveling wave tubes.

4.1.1.6 Ongoing Programs

Microwave Devices and Microwave Integrated Circuits

This technology area is not currently separately funded. Work is performed on an individual project basis and through use of corporate internal research and development funds, resulting in many non-standard sole source avionics components. A new program start in this area is recommended. Proposed milestones are listed below.

MILESTONES

FY 81

Develop a prioritized needs list in the areas of high cost, high volume, sole source, and/or unreliable microwave devices and circuits. Develop program plans, budgets, and interfaces with related programs including Avionics Components and Subsystems (AVCS) and Aircraft Equipment Reliability and Maintainability Improvement Program (AERMIP).

FY 82

Develop one or more "standard" microwave components or microwave integrated assemblies.

FY 83

Develop solid state power amplifiers.

4.1.1.7 Summary

The need for miniaturization, low cost, ruggedization, higher power, and higher frequency of operation of modern avionics is the driving force behind MIC technology. These goals must be pursued, along with a reasonable standardization program to ensure future availability of these specialized parts, preferably from multiple sources.

4.1.2 HYBRID MICROCIRCUIT PACKAGING

4.1.2.1 Background

Hybrid microcircuit packaging technology has achieved maturity during the last decade. The technology has been used in applications ranging from digital computers to analog control circuits to power switching devices. The use of the technology is, in no small part, responsible for the ability of avionic system designers to utilize small, lightweight, but very dense electrical subsystems. Hybrid microcircuit packaging is used as a medium to interconnect numerous components (i.e., integrated circuits (ICs), transistors, diodes, capacitors, resistors, inductors, and other devices) to one another in a benign, mechanically sound structure which can then be attached or interconnected to a higher level assembly. Because of this use of technology, the direction of its development is dictated by the never ceasing advancement and complexity of components, particularly digital ICs, and the system designer's demands for smaller, lighter, denser, and less expensive packages.

4.1.2.2 Current Status

Hybrid technology offers a vital tool for the mechanization of high speed custom circuits which require combinations of digital and analog circuits, and discrete passive devices in the same package. This technology also is cost-effective in certain applications, when compared to monolithic approaches, especially in the limited quantities that the military typically procures. With the advent of readily available large scale integrated (LSI) devices, such as microprocessors, memories, and other custom semiconductor

application forms, the trend in packaging will increasingly be toward smaller and lighter electronic systems; thus, emphasis must be placed upon improving the hybrid packaging technology.

Hybrid technology offers the following packaging and circuit advantages:

* small size and weight,
* economy for small production quantities when compared to monolithic circuit development costs,
* close control of circuit geometrical tolerances,
* functional trimmability,
* compatibility with most types of active and passive chips,
* increased reliability due to decreased circuit interconnections,
* thermal efficiency,
* low stray circuit capacitance, and
* increased mechanical survivability.

These attributes have allowed military system designers to use this packaging technology in radars, sonars, communications equipments, countermeasures equipments, surveillance equipments, guidance systems, computers, power systems, etc. Utilization will continue to grow as reliabilities increase and costs decrease.

4.1.2.3 Perceived Trends

Present technology trends emphasize computer-aided processes, non-Noble metallizations, radio frequency compatibility, standardization, and qualification of processes, denser circuit topologies, computer-aided testing, ceramic packages, repairability, and increases in power handling capability. These trends are apparent when documents such as the Third Annual Hybrid Microelectronics Planning Conference Report (prepared by the Electronics Subcommittee of the DOD Manufacturing Technology Advisory Group) are reviewed. Activities resulting from recent Navy research and development (R&D) or manufacturing technology (MT) funding include:

* Radio Frequency Packaging Industry Investigation
* Metallo-Organic Materials for Improved Thick Film Reliability
* High Ohms Per Square Thin Film Resistors - MT Program
* Computerized Thick Film Printer - MT Program
* Delid and Reseal - MT Program

* Acoustic Emission Package Testing

* Standardization of Hybrid Microcircuit Design Principles for Universal Artwork

* Ceramic Chip Carrier Packaging - MT Program

* Automated Hybrid Lead Assembly - MT Program

* Bumped Tape Automatic Bonding - MT Program

* Hermetic Tape Carriers - MT Program

Future NAVAIRSYSCOM hybrid microcircuit packaging technology programs will continue to follow current trends, but with sufficient foresight to anticipate new application needs. A new generation of hybrids is expected during the next five to fifteen years. These hybrids will contain LSI, very high speed integrated circuits (VHSIC), microwave integrated circuitry (MIC), surface acoustic wave (SAW) circuitry, and integrated optics (IO) circuitry. A marriage of MIC, SAW, IO, and LSI with current micro-components in a hybrid package is inevitable. In order to meet the mechanical, electrical, and optical requirements of this advanced generation of hybrids, each supporting technology, process, and material must be scrutinized to identify present and long-term deficiencies. These shortfalls must then be resolved on a timely basis.

The following is a list of supporting technologies, processes, and materials that must be considered:

* Thin film

* Thick film

* Bonding (wire, chip and substrate)

* Substrates

* Components

* Material science

* Packages

* Testing

* Inspection

* Thermal design

* Logistic Support

4.1.2.4 Areas Requiring Further Development

Current -

* Development of solder reflow techniques.

* Development of a thin film process for depositing multiple sheet resistivities on a substrate.

* Development of a computerized thick film printer having interactive graphics capability.

* Development of assembly processes including ceramic chip carrier attachment techniques, automatic ceramic chip carrier attachment equipment, automatic self-test wire bonder, automatic lead assembler, methods for automatic bonding of bumped tapes, wire bond characterization techniques and standards, and a system for the automatic polymer attachment of components.

* Development of substrate materials and processes including MIC substrates having improved parameters, thin-film flexible substrates, metal based substrates, and substrates for fine-line thick-film application.

* Development of new components such as hermetic ceramic chip carriers and methods and materials for burn-in of chips.

* Development of non-Noble metal systems for use in all phases of hybrid fabrication.

* Development of packaging programs, including conducting investigations of RF packaging needs, package delid and reseal methods, equipment and methods for laser sealing of hermetic packages, and standardized hybrid packages.

* Development of testing requirements and procedures for high density multilayer circuits, and fabrication line qualification procedures.

* Establishment of the facility requirements for a long-term chip storage bank.

Short Term (0 to 5 years) - Programs that are anticipated during the next five years include:

* Thin film programs for depositing multiple sheet resistivities on a substrate, small quantity thin film multilayer techniques, protective conformal coatings, equipment and techniques for a fully automatic thin film deposition system, active device technology, and fine line techniques for SAW.

* Development of a thick film technology, with programs for a metallo-organic ink system, techniques for fine line deposition, fabrication line qualification and certification procedures,

capacitor materials, methods for utilizing universal thick film design guides, and MIC compatibility.

* Development of assembly processes, including ceramic chip carrier attachment techniques and automatic attachment equipment, automated aluminum ball bonding techniques, automatic self-test wire bonding, acoustic emission testing of bonds and packages, automatic lead assembly, automatic bonding of bumped tapes, wire bond characterization techniques and standards, automatic polymer attachment of components, hybrid assembly techniques for MIC and RF circuits, and substrate and component solder attachment techniques.

* Development of substrate materials for MIC substrates having improved parameters, SAW including piezo-electric films on silicon, flexible substrates, metal based substrates, large area alumina substrates, and fine line thick film application.

* Improvement of hybrid components in the areas of improved chip capacitors and inductors, improved MIC devices, ceramic chip carriers, and methods and materials for burn-in of chips.

* Development of material systems and processes for non-Noble metal systems for use in all phases of hybrid fabrication, thick film hermetic glass compositions, piezo-electric thin films and crystals, epoxy characterization methods and techniques, and a hybrid monometallic system.

* Development of packaging technology in the areas of compatibility with RF circuitry, large area packages, compatibility with integrated optics, delid and reseal methods, equipment and methods for laser sealing of hermetic packages, non-hermetic packaging techniques, non-magnetic packages, localized hermetic seals, automatic package sealing techniques including parts handling, and standardized hybrid packages.

* Development of test programs and equipments such as an automatic self-programming test system, methods for testing RF and MIC hybrid circuitry, detection methods for identification of trapped particles in packages, testing requirements and procedures for high density multilayer circuits, fabrication line qualification procedures, fault isolation and diagnostic methods and principles, methods and guides for incorporation of built-in-test in hybrid circuits, equipment and techniques for automated optical defect recognition and chip assembly, infrared image inspection equipment and techniques, and automated incoming component inspection techniques.

* Development of thermal design technology in the areas of computerized thermal design, materials and mounting techniques for improved thermal dissipation from improved packages, and thermal analysis equipment and techniques.

* Establishment of the facilities for both a long-term chip storage bank and monolithic fabrication lines for high usage, obsolete chip technologies.

* Establishment of standard documentation practices.

Mid Term (5 to 10 years) - The following programs are anticipated to be required in the next five to ten years:

* Development of thin film technology in the areas of active devices, optical wave guides, and fine line techniques for SAW.

* Development of thick film technology in the areas of metallo-organic ink systems, techniques for fine line deposition, MIC compatibility, energy efficient thick film firing methods, and materials and methods for thick film optical wave guides.

* Development of packaging techniques with programs addressing acoustic emission testing of bonds and packages, assembly techniques for MIC and RF circuits, and assembly of optical circuits.

* Improvement of substrate materials in the area of SAW including piezo-electric films on silicon.

* Continuation of the development of improved chip capacitors and inductors, and develop hybrid compatible integrated optical components.

* Development of material systems for thick film hermetic glass compositions, piezo-electric thin films and crystal, and mono-metallic hybrids.

* Continue package development in the areas of fabricating large area packages and package compatibility with integrated optics.

* Development of test methods and equipment for automatic self programming test systems, test methods and equipments for integrated optic hybrid circuits, incorporation of built-in-test in hybrid circuits, continue development of equipment and techniques for automated optical defect recognition and chip assembly, continue development of infrared image inspection equipment and techniques.

* Development of thermal design technology in the areas of materials and mounting techniques for improved thermal dissipation from packages, and thermal analysis equipment and techniques.

* Establishment of additional capability to maintain monolithic fabrication lines for high usage, obsolete chip technologies.

Long Term (10 years plus) - The following programs are anticipated in the long term:

* Continue development of thin film optical wave guides.

* Continue development of materials and methods for thick film optical wave guides.

* Continue development of techniques for assembly of optical circuits.

* Continue development of hybrid-compatible integrated optical components.

* Continue development of test methods and equipments for integrated optic hybrid circuits.

* Establish additional capability to maintain monolithic fabrication lines for high usage, obsolete chip technologies.

4.1.2.5 Development Priorities

Development plans in the next five years should emphasize increased automation of all phases of hybrid packaging, characterization and qualification of materials and processes, and optimization of the technology for application to high speed digital and RF circuitry. Far-term plans should emphasize compatibility with emerging technologies such as SAW and IO.

4.1.2.6 Ongoing Programs

Several programs are currently in process relative to hybrid microcircuit packaging as shown below.

MILESTONES

FY 81	
High ohms per Square Thin Film Resistors	Feb 81
Radio Frequency Packaging Industry Investigation	Jul 81
Metallo-Organic Materials for Improved Thick Film Reliability	TBD
Computerized Thick Film Printer	TBD
Delid and Reseal	TBD

4.1.2.7 Summary

The unique capability of hybrid packaging to combine a variety of advanced technologies in a package to form a distinct functional unit which is compatible with higher order assemblies, guarantees that this packaging technology will play a dominant role in future avionic systems. Usage in the last ten years has increased dramatically as the technology has matured, resulting in many present day systems whose capabilities and even existence would not be possible without hybrid packaging. Emphasis must be placed on continuing to develop the technology to meet system needs and attain required microcomponent complexities.

4.1.3 VERY HIGH SPEED INTEGRATED CIRCUITS (VHSIC)

4.1.3.1 Background

Over the past several years, the Department of Defense (DOD) has maintained a policy of minimizing the funding for advancing the state-of-the-art of integrated circuit (IC) technology and devices for defense application in favor of utilizing the advancing commercial IC technologies. This policy was abandoned in FY 79 primarily because: (1) the U.S. lead in military applications of IC based computer technology over potential adversaries had eroded significantly, and (2) the DOD market share for ICs was (at that time) less than 7 percent of the total market, and the commercially driven semiconductor industry demonstrated increasing reluctance to respond to the stringent military needs for qualified ICs and low volume custom devices.

In order to reverse this trend, a new DOD initiative called Very High Speed Integrated Circuits (VHSIC) program began in FY 79.

The VHSIC program is a major DOD thrust to advance the state-of-the-art of integrated circuit technology in order to support the high speed, high throughput signal and data processing requirements of defense systems in the mid-1980's and beyond. This program will develop a monolithic, very large scale, high speed, integrated circuit technology which can produce complex devices in order to mechanize the critical electronic subsystems required to meet future military needs. Successful completion of the VHSIC program will enable DOD to retain and extend the U. S. technological leadership in advanced military electronics, reduce life cycle costs of military electronic systems, and insure future utilization of advanced integrated circuits in military systems. The end goal driving the entire program is to reach the capability for advanced systems based on an availability of military-qualified integrated circuits with sub-micron feature size by the mid-1980's time frame.

4.1.3.2 Current Status

The VHSIC program is divided into four parts called Phases 0, I, II, and III, each with individual goals. Phase 0, or the definition phase, consists of systems analysis, technology trade-offs and establishment of an approach to Phases I and II, and resulted in proposals for completing those phases. The primary emphasis of Phase I is the development of 1.25 micron feature size integrated circuits and will demonstrate the feasibility and applicability of design tools, simulation aids, chip design/architecture/software/testing and packaging as it applies to construction of complete electronic brass board electronic subsystems for military application. Phase II is a continuation of the program, leading to the development of high speed complex integrated circuits at the submicron feature size with increased chip density and speed which will be utilized in system demonstrations. Phase III runs parallel to the other phases and will concentrate on items such as key technology, packaging techniques, developments, equipments, design tools, etc.

In Phase I, VHSIC-1, DOD contracted for certain high-priority systems that use ICs designed around 1.25-micron design rules and military-qualified to the full military temperature range and prescribed radiation-level specifications. A fundamental aspect of the program is the development of broad usage chips in order to minimize the need for custom circuits. The

functional throughput rates must exceed 10^{11} gates/second. This figure of merit is defined as the number of equivalent gates on a chip multiplied by the clock rate. The ICs developed in VHSIC-1 must include built-in testability test circuits and/or fault tolerant designs.

VHSIC-2 will establish means to develop an advanced capability of producing militarized ICs designed around submicron rules. Once again, minimizing customization is a fundamental consideration. Built-in testability and fault-tolerance concepts are required, as in VHSIC-1. The fundamental throughput rates must be pushed up to 10^{13} gates/second. This phase includes the system demonstration of the electronic brassboard subsystems.

The third part of VHSIC, VHSIC-3, is intended to provide diverse technology efforts which are generic in nature and which are supportive of Phase I and Phase II. The majority of the Phase III contracts are of short duration (two years or less) and focus on key technical issues. Phase III contracts have been awarded in the following areas:

* High resolution lithography (11 contracts),
* Architectural and design concepts for reducing custom fabrication, increased chip utilization, minimizing signal transfer delays, and efficient system design (4 contracts),
* Architectural concepts to improve system reliability (3 contracts),
* Concepts for on-chip test capability (3 contracts),
* Computer-aided design concepts (3 contracts),
* Integrated circuit package improvements (3 contracts),
* Improved semiconductor substrate materials and fabrication processes (8 contracts),
* Analytical methods for determining substrate defects (3 contracts),
* Development of new structures for high speed signal processing (3 contracts),
* Development of new device structures for integrated circuit gates (6 contracts),
* Approaches to improve and simplify the utility of VHSIC technology (3 contracts),
* Innovative tester concepts (2 contracts), and
* Other developments to support the main VHSIC program (1 contract).

In the spring of 1980 the DOD awarded nine contracts for the Phase 0 (definition phase) to culminate in proposals for Phases I and II, due in late 1980.

4.1.3.3 Perceived Trends

The following major trends are expected to result from the VHSIC program:

* Advance the time of introduction of very large scale integrated (VLSI) circuits into DOD military systems at least five years ahead of present projections.

* Focus the IC industry on DOD needs through establishment of distinct goals and funding infusion.

* Have latest state-of-the-art devices available to DOD in advance of commercial exploitation, thereby reversing the present situation of a 2-5 year lag.

* Advance IC technology to submicron dimensions (beyond the limits of optical lithography).

* Replace 50 or more present ICs with one IC, thereby providing at least a ten-fold reduction in size, weight, power consumption and failure rate, with concomitant savings in both initial and life cycle costs of present military computer processing systems.

* Provide ICs with 100 times the processing throughput of present ICs, allowing new and important capabilities for military applications such as cruise missiles, satellites, avionics, radar, undersea surveillance, electronic warfare, etc.

* Insure a responsive continuing manufacturing base attuned to meeting DOD needs.

Specifically, the following developments are expected:

* Design and fabricate VHSIC chip sets for computation and signal processing applications at the 1.25 micron feature size with a figure of merit of 5×10^{11} gate-Hz/cm^2.

* Construct electronic brassboard subsystems (test beds) of selected avionics in 1983.

* Design and fabricate VHSIC computational and signal processing chip set with submicron (0.5 to 0.8) feature size and a figure of merit of 10^{13} gate-Hz/cm^2 by 1985.

* Selected avionic system demonstrations using VHSIC chips with submicron feature size by 1985-86 time frame.

* Devices capable of Military Specification performance.

* Develop chips tolerant of specified radiation levels.

* Include appropriate fault tolerance and built-in test design.

* Specify VHSIC device failure rates not exceeding 0.006 percent per 1,000 hours at 60 percent confidence level (end goal) both while operating and stored over the range of -55°C to +85°C case temperature.

* Develop computer-aided design (CAD) tools necessary to do top-down system to device design.

* Develop lithography equipment requirements.

4.1.3.4 Areas Requiring Further Developments

Current -

* Complete Phase 0 concept studies and proposals.

Short Term (0 to 5 years) - Areas to address in the short term include:

* System/device architecture and chip set specifications.

* System/device testability.

* Device design and fabrication.

* Lithography techniques and equipments.

* System/device testability.

* Device design and fabrication.

* Lithography techniques and equipments.

* VHSIC wafer fabrication techniques and equipment.

* Computer-aided design and manufacturing tools.

* Techniques for the timely and controlled introduction, and acquisition of devices.

* Life cycle support of VHSIC technologies in avionics.

* System software developments.

Mid Term (5 to 10 years) - Areas to address in the mid-term include:

* Introduce VHSIC technology in appropriate avionics.

* Provide for out-year device logistics support.

* Investigate Gallium Arsenide IC technology (not part of the VHSIC program).

Long Term (10 years plus) - Areas to address in the long-term include:

* A new VHSIC-type program directed towards Gallium Arsenide integrated circuit technology, if feasible (not part of the VHSIC program).

4.1.3.5 Development Priorities

Development priorities are currently being assessed in Phase 0 program definition studies.

4.1.3.6 Ongoing Programs

Program schedule and associated milestones are shown in Figure 4-5.

4.1.3.7 Summary

The VHSIC program should meet presently defined and future military systems needs while providing an increased ability, on the part of the U.S. electronics industry, to respond fully and quickly to DOD's continuing and rapidly expanding requirements for complex, high speed signal processing functions in its electronic subsystems and systems.

4.1.4 ELECTRO-ACOUSTIC DEVICES

4.1.4.1 Background

Surface Acoustic Wave (SAW) technology represents a practical form of implementation and construction of various signal processing functions covering a frequency range from 10 MHz to at least 400 MHz. SAW technology is cost effective in terms of manufacturing and maintenance costs. Devices are fabricated using conventional hybrid circuit techniques on appropriate substrate materials. SAW devices convert electrical energy to mechanical acoustic wave patterns and mechanical acoustic to electrical energy wave patterns by utilizing a piezo or ferro-electric material. Such materials include Quartz, Lithium Niobate ($LiNbO_3$), and Lithium Tantalate ($LiTaO_3$). The electro-mechanical conversion is effected by inter-digital transducers of vacuum deposited aluminum on the piezoelectric material surface. Various SAW devices can be produced by varying finger overlaps and spacings. The planar form of construction makes SAW devices compatible with hybrid microcircuits and Microwave Integrated Circuits (MICs). SAW presents increased mathematical and modeling design problems due to a time domain - frequency domain interdependence, which complicates the design process. Spatial distortion of the acoustic energy produced by second-order effects necessitates elaborate compensation techniques in order to achieve high dynamic ranges.

MAJOR MILESTONES FOR THE DOD VHSIC PROGRAM

PHASE 0

PROGRAM DEFINITION

PHASE I

PHASE Ia

1.25 MICRON FEATURE SIZE
CHIPS AND SUBSYSTEM BRASSBOARDS

PHASE Ib

SUBMICRON TECH-
NOLOGY DEVELOPMENT

PHASE II

PHASE IIa

SYSTEM DEMONSTRATIONS

PHASE IIb

SUBMICRON VHSIC DEVICES
FOR AVIONICS SYSTEMS

PHASE III

MULTIPLE CONTRACTS
THROUGHOUT PROGRAM

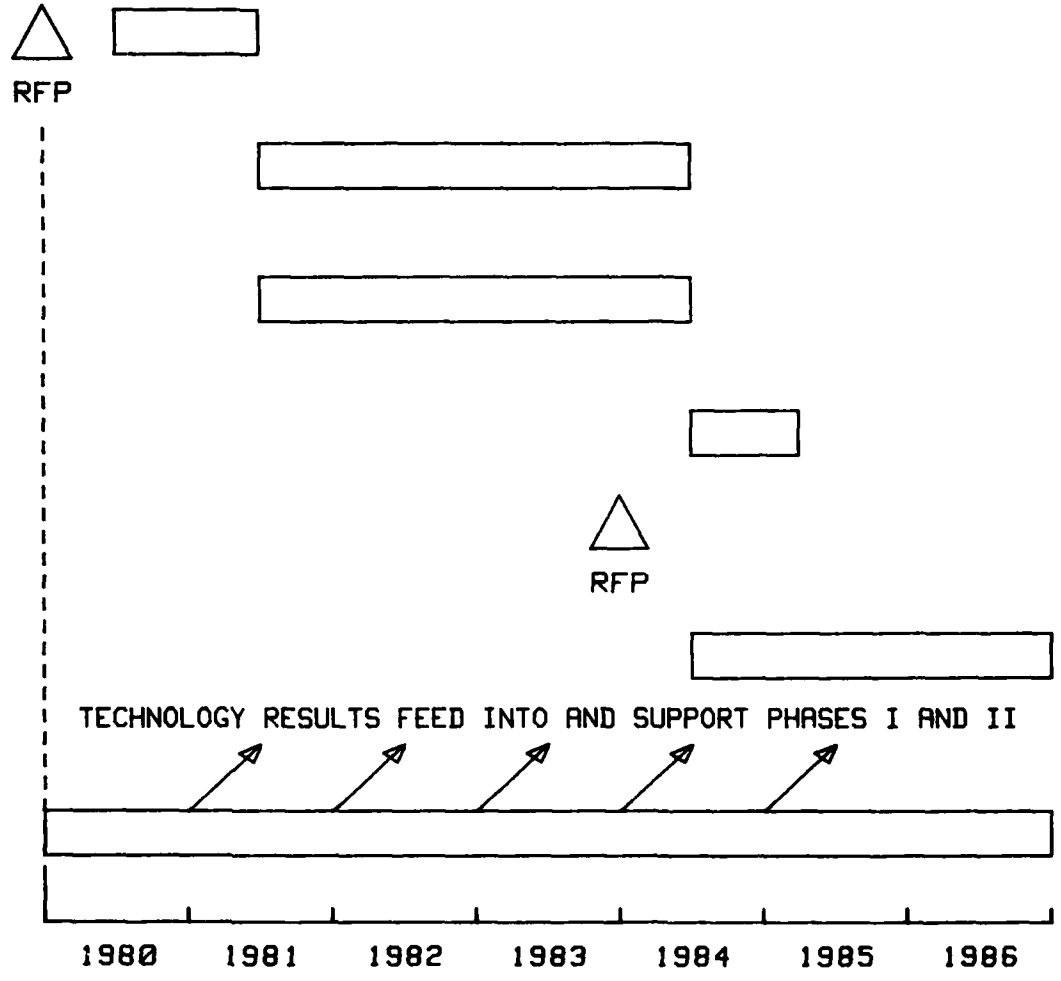


FIGURE 4-5

4.1.4.2 Current Status

SAW devices perform complex signal processing functions in real time, at high speed, in circuitry occupying less space, with less weight, and consuming less power, than most current circuit techniques.

Current commercially available SAW devices include:

* Non-Dispersive Delay Lines
* Dispersive Delay Lines
* Tapped Delay Lines
* Bandpass Filters
* Pulse Expansion/Compression Filters
* High "Q" Resonators
* SAW Oscillators
* Correlators/Convolvers
* Digitally Programmable Delay Lines
* Digitally Programmable Bandpass Filters
* Digitally Programmable Frequency Synthesizers
* Digitally Programmable Matched Filter Correlators
* Phase Shift Keying (PSK) Code Generators
* High-Speed Data Multiplexers
* Chirp (Fourier) Transform Processors

These devices can be built on SAW substrates as small as 1 cm square.

The Navy is currently funding research in the development of a SAW pressure transducer which has potential applications in jet engine controls.

4.1.4.3 Perceived Trends

SAW devices are expected to find application in many areas:

* Airborne Early Warning and Air-to-Surface Radars,
* Electronic Countermeasures and Counter Countermeasures (ECM, ECCM),

* NATO compatible Identification Friend or Foe (IFF) systems, and

* Advanced Signal Processing.

The value of SAW technology stems from its versatility and ability to implement real-time processing functions previously impractical or impossible with other technologies. SAW technology also benefits from its small physical size and weight, and a planar form of construction which is compatible with other technologies used in integrated avionics systems.

While currently available devices have a fundamental frequency limit of approximately 400 MHz, the limit is expected to pass 1 GHz and perhaps approach 2 GHz as photo and electron beam lithography resolution increases.

4.1.4.4 Areas Requiring Further Development

Current - At present, SAW research in the United States is limited to in-house and federally funded efforts for specific applications; such as specialized IF filters for communications equipment. To obtain devices for common avionics use, the Navy will be required to fund research efforts for devices which are adaptable to varying requirements, and to develop the expertise needed to reduce new device design efforts to routine procedures.

Short Term (0 to 5 years) - Photo lithographic techniques must be improved to meet the resolution requirements of SAW, such that sub-micron geometries can be fabricated. This will permit SAW devices to approach and perhaps exceed 2 GHz center frequencies.

Improved device models must be developed to reduce the number of development cycles needed to reach a final design.

Investigation of mixed technology devices such as programmable bandpass filters and programmable frequency hopping oscillators should be pursued.

Monolithic SAW-on-silicon devices should be developed using a combination of SAW, thin film, and monolithic technologies on a single silicon chip.

Limited time-length correlators/convolvers need further development to improve repeatability, reproducibility and to increase the time-bandwidth product available.

Mid Term (5 to 10 years) - Further device modeling improvements will be needed to account for higher order effects which will become limiting factors in applying SAW devices to uses requiring greater dynamic range and lower signal attenuation.

Additional research should be pursued to identify substrate materials which will permit higher device frequencies, reduce lithographic resolution constraints, and increase temperature compensation and available bandwidth.

Improved substrate material manufacturing techniques will allow larger substrates, offering economy-of-scale cost reductions for production line devices.

Continued effort will be required for developing monolithic SAW-on-silicon chips.

Long Term (10 years plus) - SAW resonators may prove suitable as inductance/reactance devices for high frequency analog electronic circuitry.

Integrated Optical Spectrum Analyzers using laser optics and SAW technology to provide real time analysis may achieve greater bandwidth, signal-to-noise ratio, and improved efficiency.

4.1.4.5 Development Priorities

Navy funding should be directed to the development of those military required devices which do not have large commercial application areas. These include programmable frequency hopping oscillators and bandpass filters, matched filter correlators, convolvers and other programmable devices.

4.1.4.6 Ongoing Programs

There are no known funded Navy programs addressing the area of electro-acoustic technology. To meet future needs of the Navy, efforts should be established to achieve the following milestones in SAW development.

MILESTONES

FY 81
Evaluate currently available devices for adaptability to Navy uses.
Identify additional applications not currently served by SAW devices.

FY 82
Fund efforts to develop devices for identified new applications.
Evaluate device model improvement potentials.

FY 83
Investigate the usefulness and practicability of mixed technology devices and monolithic devices.

4.1.4.7 Summary

SAW technology offers the ability to perform complex signal processing functions in real-time, at high speed, with circuitry occupying less space, with less weight, and consuming less power than most current circuit implementations. In particular, SAW devices will be especially suited to future airframes, where size, weight and power limitations place significant constraints on equipment designers.

4.1.5 FIBER OPTICS

4.1.5.1 Background

The use of fiber optics (FO) for data transmission is an emerging technology with much promise for the future. The application of FO technology to avionic systems in military aircraft is attractive since fiber optics exhibit almost complete invulnerability to electro-magnetic interference (EMI) and provide increased bandwidth capability over conventionally wired implementations. Fiber optics also possess a potential weight/volume advantage over conventionally wired systems.

Although there is still room for research and development efforts in FO technology, past development of components, experimental system models and FO systems concepts have shown the feasibility of using FO transmission elements in avionics systems. Past and ongoing development programs have taken FO technology to a state of maturity where it can be an advantageous approach for avionics systems design. The next step is to incorporate FO systems on operational military aircraft.

The applications of FO technology to avionic systems are many. These include point-to-point digital data links (low and high speed), digital data buses (both MIL-STD-1553 and wideband), specialized wideband point-to-point analog links, and optical sensors and transducer systems. Development in all these areas has been initiated and is continuing.

4.1.5.2 Current Status

FO developmental efforts exist in areas that range from electro-optical devices, through optical connectors and optical cables to total fiber optics data transmission systems. The systems work is concerned with development of a fiber optics version of MIL-STD-1553 technology, and optical sensor and transducer systems, as well as investigations of wideband requirements in FO systems, and an overall systems approach to FO for avionics. Concurrent with the systems work is development of the support elements required to realize an FO system. The Navy's 6.2 program for fiber optics is addressing development of optical sources and detectors, optical connectors, and optical fiber technology (radiation hardened fibers, high temperature cabling, low loss cabling, and fiber buffering). The Navy also has initiated manufacturing technology (MT) programs to support and advance FO technology. These programs have developed a number of FO components and circuit modules that can be used to fabricate FO systems. MIL-STD-1553 compatible FO modules have been developed, as well as improved sources and detectors.

The lack of a complete set of mil-approved standards and specifications for fiber optic components and test methods has limited their use for military applications. This deficiency is being addressed, and these documents should be available in the near future. At the present time, the AV-8B aircraft, with two point-to-point FO data links, is the only Navy aircraft committed to the use of fiber optics.

4.1.5.3 Perceived Trends

Extensive research and development in all aspects of FO technology are expected to continue. Whereas past development has addressed both bundle and single fiber technology, future development will concentrate on single fiber implementations. Many reliability and integrity questions about single fiber systems have been adequately answered in past developments. As the need

to update existing aircraft grows, and the trend toward totally integrated avionics suites increases, the realization that FO systems can enhance systems performance (EMI immunity, high bandwidth, lower weight/volume) will increase. This will lead to greater use of FO data buses and data links. Large scale retrofit of FO transmission lines into conventionally wired aircraft on a one-to-one basis is not expected or practical. However, the advantages of fiber optics can and will be realized if its use is specified early in the development of new aircraft, or judiciously applied to modifications for existing aircraft.

The use of optical sensors and transducer systems will expand. Often, the sensors are located in combustible areas of the aircraft and/or in areas of high RF interference. Optical sensors and fiber optics links eliminate the spark/fire hazard and result in accurate data transmission.

Overall, increased use of FO systems in military aircraft is expected. The existence of standards and specifications for FO components and systems and FO test methods will facilitate this transition.

4.1.5.4 Areas Requiring Further Development

Current and Short Term (0 to 5 years) - The feasibility of using FO techniques has been shown. The major obstacle to using fiber optics in military systems is the lack of mil-qualified FO components that can be used to build the systems. In some areas (sources, detectors, optical cables) the components exist, but the standards and specifications to purchase and qualify these are needed. This area is being addressed and the preparation of the required documents should be a prime objective.

In other areas (single fiber connectors and optical couplers) development that will result in mil-qualified components is required. Along with these two developments, investigations into optimal FO implementation of MIL-STD-1553 as well as other data buses and links should continue. This includes conversion of the AN/AYK-14(V) Standard Airborne Computer to accept a FO MIL-STD-1553 input. Systems performance and life can be enhanced with continued development in the following areas:

* Optical multiplexing techniques,
* Radiation hardened fibers,
* Low loss optical cabling,
* Fiber buffering,
* High temperature optical cabling,
* Long wavelength (1.2-1.6 micron) sources and detectors, and
* Militarized laser diode packaging.

Developments to expand the family of optical sensors and transducers should continue. As the number of available optical sensors increases, steps can be taken to integrate the sensors into an optical sensor bus architecture to handle the total loop from parameter sensing to the distribution of control data.

Mid Term (5 to 10 years) - The evolution of totally integrated avionics suites will result in multiplexed data requirements beyond the capacity of MIL-STD-1553 based data buses. The anticipated wide band bus requirement should be developed and a compatible standard wide band FO bus (architecture, data rate, etc.) established. Transmitter and detector modules should be developed to support this data bus. If the data rates dictate, development of high speed electronic interface logic circuits may also be required.

During this period, it is anticipated that the development of optical sensors and transducers will have matured to the point that "fly-by-light" concepts for aircraft flight control design can be considered.

Long Term (10 years plus) - Due to the present embryo stage of this technology, definitive development requirements for this period are difficult to predict. They will mainly be developments that will correct deficiencies and fill gaps in the FO technology that have been discovered in the previous years. The area of fiber optics is expanding rapidly with new applications constantly arising. Uses not now envisioned will emerge in this time frame, and developments will need to be undertaken to support them.

4.1.5.5 Development Priorities

The following development priorities exist for FO technology:

* Expansion and development of specifications and standards for components, systems, and test methods,
* Development of a family of militarized single fiber connectors (single channel, multi-channel, right/45° angle adapters),
* Conversion of the AN/AYK-14(V) Standard Airborne Computer to MIL-STD-1553 (FO) compatability,
* Development of low loss optical couplers,
* Continued development of support elements (Navy's 6.2 fiber optics program),
* Across the board development of optical sensors and transducer systems, and
* Development of wide band FO data transfer techniques.

4.1.5.6 Ongoing Programs

Militarized Single Fiber Connectors Development (part of Navy's 6.2 fiber optics program)

The purpose of this program is to determine the requirements for a family of militarized single fiber connectors for avionics applications and to award industry contracts for the development of these connectors.

MILESTONES

FY 81

Development of epoxyless BREECH-LOK 6-channel connector (MIL-C-38999, Series IV)

Contract period	Dec 80 - Nov 81
Hardware delivery - 4 mated pairs	Dec 81

Optical Transducer Development (part of Navy's 6.2 fiber optics program)

The purpose of this program is to determine the requirements for optical sensors and transducers for various avionics applications and to award industry contracts for development of the transducer systems. Specific parameters to be sensed include linear displacement, rotary displacement, temperature, pressure, liquid level, liquid flow rate, engine speed, and mechanical strain.

MILESTONES

FY 81

a. Development of an optical linear displacement transducer system

Hardware delivery - 5 systems	Jan 81
System Evaluation	May 81
Installation of 2 systems on T-2C aircraft	Jun 81

b. Development of a feasibility model of an optical pressure transducer system

Contract period	Nov 80 - Oct 81
Hardware delivery - 2 systems	Nov 81

c. Development of a fiber optic strain sensor

Contract period	Dec 80 - Nov 81
Hardware delivery - 12 sensor segments	Dec 81

d. Development of a high temperature fiber optic temperature sensor system

Contract period	Dec 80 - Nov 81
Hardware delivery - 1 system with 4 probes	Dec 81

Fiber Optics Specifications and Standards Revision and Development

The purpose of this program is to develop and revise specifications and standards for fiber optics components and associated test procedures.

MILESTONES

FY 81

Review of existing fiber optics specifications and standards	Jan 81
Proposed specifications for fiber optics connectors and attendant test procedures	Apr 81
Proposed specifications for fiber optics sources and attendant test procedures	Jul 81
Proposed specifications for fiber optics detectors and attendant test procedures	Oct 81

Development of Standard Test Methods for Short Distance Applications of Fiber Optics

The purpose of this contractual effort with the National Bureau of Standards (NBS), Boulder, Colorado, is to identify and verify required standard test methods for the evaluation of optical fibers/cables for avionics applications.

MILESTONES

FY 81

Background investigation of current and emerging measurement standards to identify required tests	Aug 81
Conduct tests on optical fibers/cables to verify measurement techniques	Aug 81

4.1.5.7 Summary

Fiber optics technology can be effectively applied to the design of avionics systems. FO techniques and implementation should be considered where conventionally wired systems cannot adequately satisfy system EMI requirements. The Navy should make a commitment to take full advantage of FO technologies, and to continue a dedicated development effort in all aspects of the field.

4.1.6 MEMORY TECHNOLOGIES

4.1.6.1 Background

The current trend in defense systems is toward increased utilization of software controlled digital electronics. Use of microcomputer controlled systems is increasing rapidly, resulting in increased usage of non-volatile memories, both read-only memory type devices to store fixed data (e.g. look-up tables), reprogrammable read-only memory type devices to store variable data (e.g. program software), and random-access memory for scratch pad or other volatile memory requirements. To achieve high performance in end item systems, there exists an ever increasing need for memory devices possessing high density, higher speed and lower power dissipation, coupled with improved reliability in severe avionic environments.

Non-volatile memories are required in applications where it is vital that stored information is not lost in case of power failure, since at times it is impractical or impossible to reload the memory. Use of non-volatile

memories also makes it possible to minimize overall power dissipation during standby operation and, thereby, improve the system performance. Characteristics as important as non-volatility are high MTBF (mean time between failure) and low life cycle cost.

Presently, there are at least 21 United States companies producing some form of non-volatile memory device. Thirteen of these are producing memory devices based on MNOS (metal nitride oxide semiconductor) and/or the floating state technique. Most of the commercial R&D effort is based on pin compatible replacement EPROMS (erasable programmable read-only memory) such as the 2716. The remaining eight companies are actively researching and a few are producing bubble memory devices.

4.1.6.2 Current Status

At the present, primarily seven types of devices are used to various extents in avionics applications or show excellent promise for near term use to provide non-volatile memory characteristics. These devices are as follows:

* Ultraviolet EPROM (erasable programmable read-only memory) (Also commonly known as UVEPROM or UVPROM)

* Mask programmable ROM (read-only memory)

* Fusible link PROM (programmable read-only memory)

* EEPROM (electrically erasable programmable read-only memory)

* EAROM (electrically alterable read-only memory)/BORAM (block organized random access memory) (MNOS)

* Core/plated wire

* Bubble

The salient features of these device types are summarized in Table 4-1.

Ultraviolet EPROM, Floating Gate, UV Erasable - The ultraviolet EPROM, floating gate, UV erasable technology uses avalanche injection of electrons into a floating gate silicon gate capacitor to store information. The writing is accomplished electrically. However, before writing is accomplished the chip must be entirely erased. A selective address clear is not feasible since the whole memory chip has to be exposed to the UV light. The UV erasable floating gate is restricted in its application due to temperature limitations and the need for UV erasure. These devices are commercially available in 512x4, 1024x4, 236x8, 1024x8, 2048x2, 512x8, 4096x8, 2092x8 and 8192x8 organizations. Production rates of EPROMs is extremely high. EPROMs are becoming a very high density device as densities will reach 28K in 1981.

ROMs, and increasingly PROMs, are extensively being used to provide strictly read-only memory. Core memory has generally been the means for satisfying most reprogrammable memory requirements, but recently there has been an increased use of EPROM and EAROM for these applications.

TABLE 4-1. SUMMARY OF MEMORY DEVICE CHARACTERISTICS

CHARACTERISTICS	EPROM	MASKED ROM	FUSIBLE LINK PROM	MNOS BORAM/EAROM	CORE PLATED WIRE	BUBBLE
Predominant Technology	NMOS, Limited CMOS; Floating Gate	PMOS, NMOS & CMOS (Bipoloar Disappearing)	Bipolar	PMOS/MNOS	Magnetic	Magnetic
Reprogrammable	Yes-200 write/ erase cycles	No	No	Yes-10^6 write/ erase cycles	Yes	Yes
Electrically Programmable	No	No	No	Yes	Yes	Yes
Maturity	Mature	Mature	Mature	BORAM-Mature EAROM-Mature	Mature	Not Mature for Military Applications
Density	High	High	Medium	Low/Medium	Very Low	High
Speed	Medium	Medium	High	Medium/Low	Low	Low
Power Dissipation (Per bit basis)	Low	Low	Medium	Medium	High	Low
Voltage Requirements	Low, Single voltage	Low, Single voltage	Low, Single voltage	High, Multi-voltage	High, Multi-voltage	High, Multi-voltage
High Temp Capability	Good (up to 100°C)(Data retention limited to about 20 yrs 0° to +70°C)	Variable (a few devices to +125°C, most limited to +70°C) (Data retention duration unlimited)	Excellent (up to 125°C)(Data retention duration unlimited)	Good (up to 125°C)(Data retention limited to about 10 yrs)	Fair (+71°C continuous, +95°C intermittent)(May have spontaneous bit alterations at elevated temperatures)	Fair (40°C to 75°C with proper screening)

TABLE 4-1. SUMMARY OF MEMORY DEVICE CHARACTERISTICS (Cont'd)

CHARACTERISTICS	EPROM	MASKED ROM	FUSIBLE LINK PROM	MNOS BORAM/EAROM	CORE PLATED WIRE	BUBBLE
Nuclear Radiation Resistance	Fair	CMOS: Good NMOS: Fair	Excellent	Good to Excellent	Excellent	Good
Resistance to Unintended Entries prior to Programming	Excellent	Not Applicable	Poor	Excellent	Excellent	Good
Number of Sources	Numerous	Numerous but diminishing	Very numerous	Very few	Few and diminishing	Few
Multisourcing Interchangeable Replacement Parts	High	Single source after mask fabrication	High	Low	Low	Low
Procurement Lead Time (General Trend)	Short	Long	Medium	Medium	Very long	Medium
Per Bit Cost (Military Quantities)	Low	High (Mask charge and minimum buy quantities)	Medium	Medium	Medium (may be low in very large memory systems)	Low

Floating Gate - Electrically Erasable (EEPROM) - The floating gate - electrically erasable (EEPROM) technology is in semi-production state. An 8K device is available from one manufacturer with 500ns/500 microsec read/write time. Another has recently introduced a 16K device with 250ns/30 microsec read/write times. This device should offer the advantages of UV EPROMs without the UV erasure requirement.

Significant advances by both commercial and DoD sponsors in solid state memory technology have established MNOS memories as a low cost, high speed, high density (in hybrid packages) alternative to magnetic memories. MNOS technology extends the implementation of these memories to DoD applications which require non-volatility, wide temperature range, low power and high density memory devices. The MNOS 8K BORAM (block oriented random access memory) devices are presently used in at least four DoD programs. The commercial MNOS devices are being used in applications such as radio/TV tuners, PROM/ROM and RAM replacement, and UV EPROM replacement. There were over 20 million MNOS devices produced during last year by two industry sources. A foreign manufacturer is producing a 2048x8 (MNOS) device as a UVEPROM replacement.

Core/Plated Wire - The core/plated wire technology has a very large commercial base. However, it is uncertain if core will have this advantage in 1990 since semiconductor (volatile) memories are being accepted by large computer makers. Core uses destructive read-only (DRO) read out, which in some cases is undesirable. The primary reason for core memories surviving this long is due to the unavailability of non-volatile semiconductor RAMs.

Plated wire technology has been mainly developed by and for DoD programs/systems that require non-destructive read-only (NDRO), high MTBF, and nuclear radiation tolerance. This technology is expensive since it does not have a good commercial base. By 1985, there will be only one, or perhaps two, suppliers of plated wire left in the United States if the technology is only used by the DoD.

Magnetic Bubble - Magnetic bubble memory is in the development stage and is inherently a non-volatile, low power device. The technology is ready for feasibility testing, and has good potential and application in the commercial world. The bubble memory is being developed by eight companies. Two source 256K bubble memory devices have been characterized at various electrical and temperature conditions. Some commercially developed devices, while designed to meet -10°C to 70°C temperature range, require temperature screening of all the units. The following device organizations are commercially available: 256Kx1, 512Kx1, 512Kx2, and 1024Kx1. At this point, bubble memory technology is not a stand alone technology but requires external integrated circuits to perform control functions.

RAM (random access memory) is usually either provided by core, or semiconductor RAMs in either bipolar, NMOS (N-channel metal oxide semiconductor) or CMOS (complimentary metal oxide semiconductor) technology. PMOS (P-channel metal oxide semiconductor) technology is rapidly disappearing from the marketplace in other than special extremely high volume commercial applications. Bipolar devices offer optimum switching speed and excellent gamma radiation hardness. CMOS devices offer minimum power dissipation and high noise immunity. NMOS RAMs offer high density and are available in both static

and dynamic versions. Presently, the dynamic memory devices can not meet all classes of MIL-E-5400 temperature requirements although testing indicates -55°C to +85°C capability in present militarized 16K devices. The militarized, dynamic 16K device, requires refresh circuitry, but presently provides the optimum in high density and reduced power dissipation in the standby mode. The advent of the 64K bit NMOS dynamic RAM has severely impacted the CCD (charge coupled device) technology efforts. Certain manufacturers eventually hope to offer 64K dynamic RAMS in full military temperature range.

4.1.6.3 Perceived Trends

Memory developments are a fast moving technology. Densities are increasing rapidly. Dynamic RAMs in 64K density are beginning to enter the marketplace and will eventually make obsolete the 16K devices commonly used today. On-chip refresh will ultimately be added to make such devices appear static to the user. CMOS RAMs are reaching 16K density. Masked ROMs are presently growing to 256K and are anticipated to reach 1 megabit by 1983. EPROMs, currently available in 64K density, are expected to reach densities of 128K in 1981 and 256K in 1982. Magnetic bubble memories have reached 1 megabit density, but presently have very limited avionic applicability due to limited temperature range (0 to 70°C maximum), slow operating speed (to about 200 KHz), and lack of second sourcing. To achieve the very high densities, VLSI (very large scale integration) technology with sub-micron dimensions will be utilized, along with on-chip fault tolerance, built-in-test and error detection and correction. Other improvements, such as improved speed and lower power dissipation, are occurring in existing device types. The sharp distinction in characteristics between bipolar and MOS (metal oxide semiconductor) devices is gradually being reduced as manufacturers improve density and reduce power dissipation in bipolar devices and increase speed in MOS devices.

New devices are also entering the market place. Of particular interest is the EEPROM (electrically erasable programmable read-only memory) which is somewhat similar to EPROMs, but can be erased electrically, thus eliminating the extensive logistics problems associated with ultraviolet (UV) erasure. Some manufacturers are indicating 100,000 read/write cycle capability. Densities are presently low (about 8K maximum), but will likely grow. This device could ultimately have considerable avionic application in providing non-volatile, electrically controlled read/write memory.

Further downstream, beyond silicon technology, GaAs (gallium arsenide) is perceived to have potential for densities of 1 gigabit, switching time of less than 100 picoseconds and capability for very high temperature application. GaAs memories are projected to be five to ten years in the future for significant availability of commercial devices, and probably greater than ten years for militarized devices.

The entire memory market is steadily growing in yearly sales with dynamic RAM representing the largest dollar value and fastest growth rate.

4.1.6.4 Areas Requiring Further Development

Current Deficiencies - A distinct need exists for an improved militarized, high density memory for providing non-volatile RAM, or at least

read-only memory with in-circuit reprogramming capability. The current device baseline for such applications is core memory, which represents a low density aging technology and is apparently responsible for a high number of equipment failures in the Fleet. EPROM is being used to replace core in certain reprogrammable applications, but this type of device necessitates a very inconvenient UV erasure cycle and has limited high temperature capabilities. EAROMs provide in-circuit, completely electrical, reprogramming, but are presently characterized by such disadvantages as difficult metal nitride processing, low density compared to other semiconductor memories, low speed, multi-voltage drive including voltages higher than normally otherwise available in either digital or analog electronics, limited sources of interchangeable parts and high per bit cost. Hence, avionic application has been limited.

Short Term (0 to 5 years) - The following action should be undertaken to increase the availability of memory devices suitable for avionic application.

* Conduct a program to characterize, qualify and standardize a family of high density EPROMs suitable for avionic application. Multisourcing of interchangeable parts should be strongly considered in selecting device types for this program.

* Conduct investigative tests and MT (manufacturing technology) programs as applicable to determine the feasibility of improving EAROMs and bubble memory in their respective areas of difficiencies to make them suitable for widebased applications in avionic systems to provide the needed in-circuit, non-volatile reprogrammable read/write memory device to replace core. Particular attention should be given to bubbles because of their very high density, resistance to nuclear radiation, and low per bit cost.

* Investigate EEPROMs, and their potential for providing this same capability. Initial indications are seemingly quite favorable for application of this type device.

Mid Term (5 to 10 years) -

* Based on the results of the short term investigations, determine the device type(s) to be established which will provide the required reprogrammable memory (either EAROM, bubble or EEPROM).

* Conduct a program to characterize, qualify and standardize a family of such devices and develop adequate multisourcing of interchangeable parts suitable for broad based avionic applications.

* Investigate and/or develop GaAs technology memory and determine its applicability to avionic applications. Particular emphasis should be placed on establishing reliable, repeatable GaAs processing techniques.

* As Josephson devices (a device based on superconductivity which must be maintained near obsolute zero (-273°C) temperature) become commercially available in the mid 1980s, determine the degree of applicability of these extremely high speed devices to specialized avionics applications.

Long Term (10 years plus) -

* Assuming GaAs technology memories prove desirable for providing a very high density and very high speed memory, conduct a program to put in place a family of multisourced, militarized GaAs memories.

* If the Josephson device appears to have significant avionic applicability based on the results of the mid-term effort, establish a family of militarized devices.

4.1.6.5 Development Priorities

* Priority 1 - Establish a family of fully characterized, multisourced, militarized EPROMs for immediate avionics application.

* Priority 2 - Develop and establish a family of militarized, multisourced devices (either bubble, EAROM, or EEPROM) with characteristics compatible with avionics applications, which are non-volatile and can be electrically reprogrammed within a circuit.

* Priority 3 - Develop GaAs memories.

4.1.6.6 Ongoing Programs

Information Storage and Retrieval (P.E. 62721N)

The purpose of this task is to investigate, evaluate, and validate new memory techniques and concepts to determine their applicability to future Navy avionic systems. Emphasis will be placed on determining the feasibility of adapting industry-generated concepts to Navy applications.

MILESTONES

FY 81

Complete T&E of Air Force Developed Bubble Memory Verification Hardware and Report Results	Dec 1980
Report on Cross-Tie Memory Device Architecture Study	Dec 1980
Complete Characterization of MNOS BORAM Device and Report Results	Jan 1981
Complete Phase 2 Bubble Memory Device Characterization and Report	Jan 1981
Report on Demonstration and Evaluation of Solid-State Recorder in Avionics System Test Bed (NATC Effort)	Jun 1981
Report on Fault-Tolerant Memory Concept Evaluation	Sep 1981
Complete Cross-Tie Memory System Architecture Study	Sep 1981

FY 82	
Initiate Phase 2 of Solid-State Recorder Technology Evaluation	Oct 1981
Contract for Cross-Tie Memory Technology Evaluation	Dec 1981
Contract for Memory Technology Evaluation in Support of Microprocessors	Jan 1982
Contract for Intelligent Memory/Techniques/Technology Evaluation	Feb 1982
Report on T&E of Solid-State Recorder Verification Hardware	May 1982
Report on Cross-Tie Memory Verification Hardware	Sep 1982
Report on Solid-State Recorder Technology Evaluation	Sep 1982
Publish Memory Assessment Report	Sep 1982
FY 83	
Report on Memory Technology Evaluation in Support of Microprocessors	Oct 1982

4.1.6.7 Summary

Memory is an area of rapid growth in both technology and sales volume. As avionic systems become increasingly more complex and, hence, rely more heavily upon microprocessors/microcomputers, the role of memory takes on increased importance. Emphasis must be placed upon establishing memory types consistent with the requirements of the avionics community, particularly non-volatile, high density, electrically reprogrammable devices to ultimately replace magnetic core memories.

It is clear that the Japanese are now leading in the production of high performance 16K bit N-channel MNOS EAROM memory devices that are tailored for the UV EPROM replacement market. The United States supplier has characterized this device and found it to be excellent and well within the announced specifications. The MNOS 8K BORAM memory technology/devices have transitioned to production and are being used in a few DoD information processing systems and crash recorders. The commercial MNOS EAROM devices are being produced mainly for point of sale terminals.

4.1.7 DISPLAY TECHNOLOGIES

4.1.7.1 Background

The critical nature of aircraft controls and displays has been brought into focus by the trend to smaller cockpits, reduced crews (often only the pilot) and the increasing complexity of airborne weapon systems. Subsystems and functions such as Flight Control, Navigation, Communications, Engine/Airframe performance, Threat Analysis, Countermeasurues, Weapon Selection and Delivery, Radar, Infra Red (IR), Low Light-level Television (LLTV) and Life Support are all competing for the pilot's attention (usually through visual displays). More and more equipments developed for aircraft have built-in-test capability, further increasing the information available to the crew. In the F/A-18, the major Fighter/Attack aircraft of the late 1980's and 1990's, the pilot must manage the weapons system as well as pilot the aircraft.

4.1.7.2 Current Status

The F-18 cockpit, which has been optimized for one-man operation, represents the current status of aircraft display systems. It incorporates multifunction Cathode Ray Tube (CRT) displays that minimize operator controls. Although the F-18 display system incorporates many desirable features, the goals of flexible, all purpose interfaces, and modularity of both hardware and software have not yet been achieved. The Navy Advanced Integrated Display System (AIDS) and the Air Force Digital Avionics Information System (DAIS) programs are attempting to address these goals. The latest developments in Heads-Up-Display (HUD) use holographic lens technology, which allows non-planar image surfaces. This development can increase the pilot's field of view, while also reducing the required volume for the optics and maintaining adequate brightness/contrast.

A Tri-Service integrated controls and displays activity was initiated by a Memorandum of Agreement (MOA) in July 1979. The following areas were covered by the agreement:

* Pilot Interface

* Technology
  - System Architecture
  - Display Indicator

* Interface
  - Digital
  - Video

4.1.7.3 Perceived Trends

Fewer dedicated displays and instruments will be found in future/updated aircraft. Multifunction displays and controls will fill available panel space. Instead of dedicated controls, programmable displays (perhaps with touch sensors) will be used. Techniques to activate these controls and change modes without requiring the pilot to take his hands off the throttle and stick will be pursued. Voice recognition of control commands (especially for the setting of numbers, i.e. radio frequencies, navigation headings etc.) is one such technique; another is an eye tracking system to "look at" and activate the controls.

Display systems will include powerful processors which will be made possible by VHSIC and other advancements in integrated circuit technology. These processors will generate real-time, three-dimensional graphics, convert sensor formats into display formats, perform image enhancement algorithms, and perform alignment and registration of multiple image sources and/or stored images to create real-time overlays.

A tremendous opportunity exists to reduce future display system costs as the multifunction capability becomes a requirement on all Navy aircraft. Display systems will be implemented with modular building blocks and powerful standard interfaces covering both hardware and software. The pay offs will accrue in several ways: The first relates to the logistics advantages of procuring and sparing fewer unit types and the economics of scale on

purchases. Second, costly obsolescence can be avoided by addition of modules and/or appropriate building blocks. Also, technology improvements may be inserted more rapidly. To make this possible, a display system interface simulator should be available as Government Furnished Equipment (GFE).

Display management will become very complex as the goals of multi-function displays and controls are realized. To manage the task of displaying the desired information at the correct time, in an uncluttered and functional format, will require development of a display controller with a sophisticated software executive system. Software configured to support this complex task must be developed, using a high level language such as ADA. A simulator capability must be developed and maintained to develop and verify control procedures and display formats.

Although several flat panel technologies may soon become viable alternatives to alphanumeric displays, CRT's will continue to dominate the near and mid-term period for general purpose displays. Color displays should find their way into aircraft, adding another dimension to the ways of presenting information. Liquid Crystal Displays (LCD) are currently being integrated to semiconductor driver arrays in order to produce a display with each element programmable. Likewise, advances in drive circuitry are promising brighter, matrix addressable Thin Film Electro-Luminescent (TFEL) displays. Though these technologies may provide very good alphanumeric panel displays, solutions to the very limited gray-scale capabilities have not yet been found. As they are developed, better display devices should be incorporated as replacement blocks in the building block approach.

4.1.7.4 Areas Requiring Further Development

Short Term (0 to 5 years) -

* Investigate available/developmental general purpose control display unit with touch sensing for Communications, Navigation and Identification (CNI) functions for purposes of possible standardization.

* Develop efficient formats for display of engine and airframe parameters.

* Assess/Influence benefits of VHSIC and new technology on display systems.

* Develop both hardware and software with standard interfaces for display architectures.

* Develop plans for display configuration management.

* Develop planning for GFE display systems for support of other subsystem acquisitions.

* Improve HUD to have the field of view more compatible with the associated weapons systems.

Mid Term (5 to 10 years) -

* Apply VHSIC technology to basic display systems.

* Develop voice recognition techniques for control commands and integrate these with displays and back up controls.

* Apply VHSIC and VLSI to processing stored images into registered overlays for real time images.

Long Term (10 years plus) -

* Use computer graphics to provide model visualizations based on data from multiple sensors, JTIDS and intelligence data.

* Develop all-weather computer graphics carrier landing aids that receive data from radar, IR and other sources.

* Develop eye tracking systems to designate/activate controls visually.

4.1.7.5 Development Priorities

A high priority must be placed on the development of an integrated approach to display systems for the next generation aircraft, and for phase-in to current aircraft undergoing CILOPs. To achieve the goals of the integrated display, the technology of the VHSIC program and the software capabilities inherent in the ADA higher order computer language will be required. Therefore, a sustained effort to utilize the outputs of these programs must begin in the near term. An advanced architecture must be developed and standard interface definitions and controls must be an early product of these efforts.

Advanced display systems laboratories should be set up with the following capabilities: 1) Display Device Evaluation - Set up/measurement capabilities for resolution, brightness/contrast and evaluation of the suitability for applications and environment, 2) Simulation - Establish capability to simulate display formats and techniques using general purpose displays and simulate mission scenarios, and 3) Breadboard/Brassboard Development - Initiate breadboard/brassboard development of key portions of display system architectures and interfaces.

New, promising display devices must be sought out and developed for applications in the mid and long term periods.

A flexible command display unit should be developed. Several CILOP and update programs require improvements in this area. This development should be undertaken with a view toward the overall integrated display goals.

Integration of voice recognition and displays should be undertaken. A feasibility evaluation of equipment designed to sense where the pilot is looking to provide hands-off control of other equipment is also needed.

Implementation of three-dimensional computer graphics and image registration techniques for overlays should be completed during this period.

4.1.7.6 Summary

Traditionally, each subsystem, weapon system and instrument had its own dedicated displays and controls. Separate displays and controls are no longer feasible on the next generation aircraft, and multifunction advanced display systems must be employed. Further, as current generation aircraft undergo CILOP and other major updates, many of these aircraft will be excellent candidates for advanced display systems, because of the need resulting from additional sophisticated equipment.

Life cycle economies should be realized with the utilization of advanced display technologies, since the building block systems approach will allow the tailoring of displays and controls to fit the requirements of many aircraft types, and will avoid total obsolescence by addition/substitution of functional building blocks and/or selective replacements.

4.1.8 MICROPROCESSOR CONTROL

4.1.8.1 Background

Over the past two decades, digital computers have become an integral component in virtually all avionic systems. In 1961, NAVAIR maintained an inventory of only two different types of airborne digital computers. Today, an inventory of 14 non-standard, four designated standard, and five defacto standards is maintained. The widespread utilization of digital computers and the trend towards distributed architectures is creating a need to develop subsystem processors and processing elements. Subsystem processors can be utilized effectively for dedicated computational tasks, mode control, digital signal processing, filtering, analog-to-digital and digital-to-analog conversion, thresholding, and logical operations. Data can be transmitted between the mission computer and the subsystem processor over standardized interface lines such as the MIL-STD-1553 or a fiber optic digital data bus. Present day state-of-the-art microprocessor technology is being applied to the design and development of new avionic subsystem processors and processing elements. The resulting designs will feature low power dissipation and will enhance the reliability and maintainability of new equipment designs.

4.1.8.2 Current Status

The application of microprocessor technology to avionic system design is being implemented by adapting microprocessor designs developed for commercial applications. This approach is very effective in satisfying the requirement for any one particular task. However, the proliferation of micro-

processor families makes the uncontrolled application of microprocessor technology a potential logistics nightmare that results in higher avionics system life cycle costs (LCC). The utilization of existing microprocessor technology must be controlled via the imposition of hardware, language, and interface standards. These steps are necessary because the microprocessor industry is not generally oriented towards meeting the Department of Defense's (DOD's) current or future needs. The industry is geared towards satisfying the requirements of high volume commercial applications such as electronic games, appliance control and automotive controls. The first step in imposing a standard language has been completed by developing ADA, the standard DOD programming language.

Three microprocessor chips have been JAN qualified, the 8080A, the Z80 and the 9900. The 8080A and Z80 are fabricated using N-channel Metal-Oxide Semiconductor (NMOS) technology and the 9900 is fabricated using Integrated-Injection Logic (I^2L) technology.

For applications too complex to be handled by the 8-bit 8080A and Z80, there are a number of 16-bit microprocessors that have not been JAN qualified that may be utilized.

The Z8000, 8086, and 9900 have been evaluated for performance and ease of software development in a typical Naval avionics application. Preliminary results indicate that the Z8000 is well suited to such applications, especially if the arithmetic co-processor is utilized. Other 16 bit microprocessors will be evaluated in the future.

As of November 1979, there was a total of 58 general purpose microprocessors available using 4, 8, 12, and 16 bit word lengths. In addition, there were 104 single chip microcomputers available in the commercial sector. A microcomputer chip is a microprocessor chip that includes Random Access Memory (RAM), Ready Only Memory (ROM) and a limited Input/Output (I/O) capability. These quantities clearly indicate the magnitude of the logistics problem that can be created if the military were to indiscriminantly apply evolving microprocessor/microcomputer technology to avionics system design. Further, this plethora of microprocessors and their many support circuits has resulted in many differing hardware and software architectures. While this diversity offers the system designer many options, it has made standardization very difficult. Further, the availability of militarized, second-sourced components has been slow. This is particularly true of the many microprocessor support chips such as parallel and serial input/output, timers, Direct Memory Access (DMA) controllers, memories, and others. Also, the rapid advance of these technologies endangers the life expectancies of numerous product lines.

A small set of existing commercial microprocessors and microcomputers should be designated in the near term as Navy standards and microprocessor/microcomputers use will be restricted to that set. It is not possible to choose a single processor for this purpose, due to different word lengths, power/performance trade-offs, functional orientation, support requirements, etc. In fact, it is unlikely that it will ever be possible, or even desirable to restrict microprocessor/microcomputer use to a single chip

type. Similarly, an existing commercial HOL, probably Pascal should be designated as an interim standard HOL for microprocessers. Most widely available microprocessers have commercially available Pascal compilers. Due to implementation differences, transportability between Pascal compilers will be limited, but it will still represent an improvement over current practice. If a managable set of microprocessors is selected, it will be possible to develop code generators for ADA and integrate them into the MTASS system. It is likely that the manufacturers of many of these processors will also develop ADA compilers for use on stand-alone microprocessors development stations. Hopefuliy, the DOD ADA certification program will ensure that source code is transportable among these systems.

The distinction between "hardware-intensive" and "software-intensive" microprocessor applications must be definitized and applied to developments, particularly with regard to documentation. In either type of application, software disciplines must be employed during the development stage, but reduced documentation and support requirements should be applied to applications which are truly hardware-intensive.

The total impact of microprocessor technology on avionic system design will not be felt for some time. As the need for smaller, lighter, and higher performance processors increases, microprocessor technology will be increasingly applied.

4.1.8.3 Perceived Trends

Microcomputers will be employed increasingly in avionics subsystems currently connected via the aircraft's multiplexed buses, as well as other various independent equipment. The former applications would include the heads-up displays, various positional and navigational indicators, inertial navigation, air data computer, armament control, radar sets, and flight data recorder. The latter subsystems would include flight, air inlet, engine controls, and weapons systems. Further, both monitoring and built-in-test of both avionic and non-avionic equipment and functions will be enhanced by employment of microcomputer-based sensing and control electronics.

The use of microcomputers in a hierarchical computer network will best enhance the aircraft and mission capabilities. This architecture will allow assessment of subsystem information by a higher level computer or computers tasked with overall mission and aircraft control. Likewise, the higher order processors will update the subsystem tasks as the situation requires.

The implementation of distributed processing concepts will enable a group of microprocessors to perform the functions of a subsystem minicomputer, at reduced cost and with enhanced fault tolerance.

Integrated circuit fabrication technologies are yielding faster and denser microprocessor and microcomputer devices. This trend will continue, using scaled N-channel Metal-Oxide Semiconductor (NMOS) and High-Performance NMOS (HMOS) techniques. The ongoing VHSIC technology program will develop

technology and deliver products to the military for which there will be limited commercial need. These devices will be more complex and will feature very high speed signal processing with an established performance goal of 10^{13} gate-Hz/cm^2. The VHSIC program also focuses attention in other areas not presently addressed by the commercial industry. Emphasis is being placed on achieving new architectural concepts and providing chip self test, self check and fault tolerant techniques to provide reduced logistics costs to the military. The first phase of the VHSIC program is to develop 1.25 micron line width features. The second phase is to employ sub-micron geometries in both data and signal processing subsystems. One of the VHSIC program goals is an NMOS structure of 150,000 gates in one square centimeter, operating at a 30 MHz clock rate. There will be increased offerings of both microprocessors and support functions using HMOS and NMOS technologies. Processors with 32 bit widths will become available, and memory densities of both random access and read only memories will at least double. Of special value to avionic applications will be arithmetic processing units of increased performance, as well as processors dedicated to analog control, acquisition, and signal processing.

The selective-oxidation, silicon-gate Complementary Metal-Oxide Semiconductor technology (SOCMOS) will probably replace the once promising silicon-on-sapphire CMOS technology (SOS/CMOS). This technology will result in high performance, low power, radiation hard devices. This will allow implementation of radiation resistant microcomputers.

Emitter-coupled logic (ECL) is declining in popularity, although it is anticipated that oxide-isolated ECL will continue to be used for some time. Currently, no microprocessor-like devices are available in this technology, but it is probable that they will appear, on a limited basis, for those applications that demand the speed performance.

In the late 1980's and early 1990's, technology will yield components of much higher densities and speeds, as well as a wider selection of environmentally rugged products. Gallium Arsenide Field Effect Transistor (GaAs FET) technology may be responsible for the more significant improvements, particularly speed.

4.1.8.4 Areas Requiring Further Development

Current - To keep overall LCC low, the Navy should continue to utilize general purpose microprocessors wherever feasible, and should select a microprocessor family that can be utilized as the basic building blocks for subsequent avionics system designs. This standard microprocessor family could then be coupled with different combinations of RAM, ROM, or other processing chips to provide the necessary system or subsystem capability. In addition to a general purpose microprocessor, the Navy should take advantage of present state-of-the-art technology in other areas, including arithmetic processing units and programmable signal processing chips.

The environmental and availability problems with microprocessor components pose a potential problem to the employment of microcomputers in avionic systems. Consequently, military funding of selected microprocessor families could be beneficial to achieve earlier implementation of more reliable and sophisticated avionics equipment.

Short Term (0 to 5 years) - Standards for software design and documentation, hardware usage (i.e., microprocessor families, etc.), software usage and interface requirements must be developed.

Mid-Term (5 to 10 years) - Microcomputers must be implemented in avionic subsystems using predefined hardware and interface standards. Initial VHSIC components (greater than one micron feature types) should be designed into and deployed in avionic subsystems.

Long Term (10 years plus) - Military specified, sub-micron structured VHSIC data and signal processors should be incorporated in avionic systems.

4.1.8.5 Development Priorities

Development of both software and hardware standards including interfacing must be achieved.

Emphasis must be placed on environmental abilities and second sourcing of selected microprocessor product lines. In the short term, the use of industry accepted families is preferable to units solely specified by the military. This will substantially reduce the cost of documentation and support hardware and software as well as offer more application oriented solutions to avionics designers.

4.1.8.6 Ongoing Programs

Microprocessor Applications to Avionics (P.E. 62721N)

The purpose of this task is to address microprocessor technology in the areas of fault-tolerant architectures, software transportability, to recommend standards through high level language support, and to establish guidelines and recommend standards for efficient, reliable, and cost-effective use of microprocessors in state-of-the-art avionic processing systems.

MILESTONES

FY 81	
Evaluate Motorola 68000 16-bit Microprocessor	Jan 1981
Evaluate Experimental Distributed Microprocessor Subsystem	Feb 1981
Evaluate Portability of Existing System Programming Language	Apr 1981
Extend Software Portability Concepts to FORTRAN or PASCAL	Aug 1981
Implement and Evaluate Processor Fault Tolerant Concept	Sep 1981
Perform Fault-Tolerant Studies for Bus Failures	Sep 1981
Update Microprocessor Guidelines/Standard Report as Required	Sep 1981
FY 82	
Develop and Evaluate Portable Run Time Interface for FORTRAN or PASCAL	Jan 1982
Define Requirements for Fault Tolerant Bus Structure	Jun 1982
ADA Compiler Analysis and Portability Concept Extension to ADA	Sep 1982
Integrate and Evaluate Fault-Tolerant Shared Memory	Sep 1982
Update Microprocessor Guidelines/Standards Report as Required	Sep 1982

FY 83

Host ADA Compiler on Selected Computer System	Mar 1983
Integrate and Evaluate Fault-Tolerant Bus Concept	May 1983
Initiate Laboratory Model Development of Fault Tolerant 16-bit Microprocessor Architecture	Jul 1983
Develop ADA Code Generator and Support Software Tools for Selected Microprocessor	Sep 1983
Update Microprocessor Guidelines/Standards Report	Sep 1983

4.1.8.7 Summary

The sophistication and reliability necessary to future avionic requirements must be served through extensive microcomputer implementations. These applications dictate a reliable (and redundant) hierarchical bus structure.

Standards must be implemented to achieve successful design, implementation, documentation, and maintenance of microcomputer controlled avionic systems.

The diversity of needs in aircraft electronics should allow for use of several microprocessor architectures, but environmental and second source considerations must be the prime director as to suitability.

In the mid to long term, it is anticipated that many avionics subsystem designs will be able to incorporate the military specified VHSIC components.

4.2 TECHNOLOGY APPLICATION AND OBSOLESCENCE

4.2.1 Background/Current Status

In the era of the 1950's and early 1960's, DoD provided large amounts of development capital to the burgeoning semiconductor industry. This investment achieved fruition with the development and high volume production of complex diodes, transistors, and integrated circuits. During those early and formative years, DoD was a large consumer of these advanced devices and thus held a tremendous technological and market leverage, the type of leverage it still wields in the military airframe area. What was not forecast, however, was the rapidity with which this favorable market share would dissipate. As recently as 1973, DoD, through government contractors, purchased one-tenth of the semiconductor devices sold in discrete form. In 1977, this figure had dwindled to just two percent and current projections forecast DoD's share of the semiconductor market to be well below one percent. Since the DoD's semiconductor quantity requirements are small, military semiconductor product lines are much less profitable to the large semiconductor houses than those utilized in high volume, consumer-oriented products.

Recent technological advances have led to electronic industry "breakthroughs" in key areas such as very large scale integration (VLSI), surface acoustic wave (SAW), and microwave integrated circuit (MIC) devices. VLSI has created many diverse, high volume consumer markets. SAW and MIC circuitry are seeing applications in TV tuners, cable TV amplifiers, and other forms of consumer communications equipment. Integrated circuit (IC) struc-

tures containing a million devices on a single chip are predicted by the year 1985. These complex devices will continue to reduce the cost of electronic circuitry and will lead to exciting advances in futuristic consumer applications. The DoD initiated Very High Speed Integrated Circuit (VHSIC) program is projected to provide Military application components of sub-micron geometry in this same time period, although the total number of devices required to satisfy military applications will remain small compared to the commercial segment.

To remain competitive in the high volume consumer product market, each IC producer must provide his products at lowest cost, highest performance and reliability, and on schedule. In accomplishing this, each company places corporate assets in those product applications which promise the greatest economic return. The semiconductor producer must also be aware of the offerings of this competition. Should a competitor introduce a newer product that offers faster processing speeds, is less expensive, or requires less energy, that product may capture a market position that will make his original device unsaleable, and thus obsolete. Recent years have seen significant competitive inroads made by foreign IC companies selling devices to large automotive companies. This will cause domestic suppliers to seek new or more sophisticated device designs and technology processes, hence accelerating the rate of technology obsolescence and subsequent production abandonment. Current mature IC technologies have projected lifetimes of approximately seven to ten years. In the future, this life span may shrink to one to two years.

What must be realized by Navy equipment design, development, acquisition, and logistic support personnel is that by the time new avionic equipments are deployed, certain advanced electronic technology devices may already be out of production. Several bipolar technologies such as RTL (resistor-transistor logic) and DTL (diode-transistor logic) have vanished in the past years and TTL (transistor-transistor logic) is rapidly being replaced by low power Schottky TTL. Likewise, several forms of PMOS (P-channel metal-oxide semiconductor) technology have become obsolete as illustrated by Figure 4-6.

A graphical representation of the effects of accelerated technology on avionics equipment life cycles is depicted in Figure 4-7. This figure shows that equipment development and qualification cycles last four to six years, production cycles seven years, and Fleet utilization as many as thirty years, in certain applications. If vacuum tubes were chosen for a circuit design in 1945, it was not until approximately 1975 that these elements became obsolete and thus unavailable for new production, spare parts, and future mobilization needs. In stark contrast, a custom military PMOS LSI IC device, designed and produced in 1972-1973, may be unobtainable today in quantities necessary to support spare parts and future production. Thus, the devices are essentially obsolete during the time of equipment production, causing potential subsequent redesign, requalification, and associated cost and schedule impacts.

To further complicate the situation, current Navy electronic systems are mechanized with microcircuit products produced by myriad suppliers with various manufacturing technologies, and our present configuration control processes do not allow us to identify which technologies (PMOS/metal gate process, complementary metal-oxide semiconductor (CMOS)/silicon gate double-

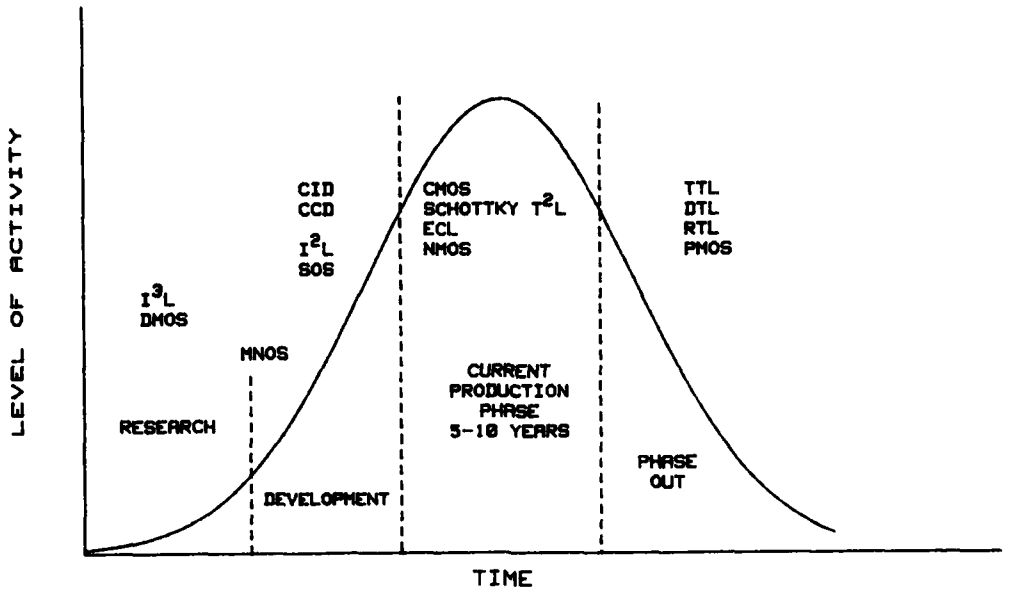


Figure 4-6. IC Technology Life Cycles

guarded process, etc.) are employed where (i.e., A7, A6, LAMPS) to do what (i.e., A7 navigation system, A6 central computer, HARM guidance system). As a result, we are typically not aware of a potentially serious procurement delay and the need for significantly increased levels of production and/or logistics funding until a few weeks or months after the needed parts are ordered and the supplier becomes aware that he cannot purchase the necessary high technology parts from the manufacturing source for support of his production.

This technology time compression and associated obsolescence phenomenon is forcing the development and utilization of new Navy controls and disciplines concerning platform and system readiness issues, availability of spares, future production requirements, and potential mobilization needs.

4.2.2 The COMPRESS Program

For the reasons stated above, the COMmercial PRoduction of Electronics Solid-state Systems (COMPRESS) program has been established and is currently planning, developing, formulating and implementing initial management policies, controls, procedures and necessary technology developments to facilitate the timely introduction, management and lifelong support of advanced electronic technologies in NAVAIR avionics.

The COMPRESS program objectives are to plan and implement management policies, controls, disciplines, procedures, and necessary microcircuit technology developments to facilitate the timely introduction, management and

EFFECTS OF TECHNOLOGY ON AVIONICS EQUIPMENT LIFE CYCLES

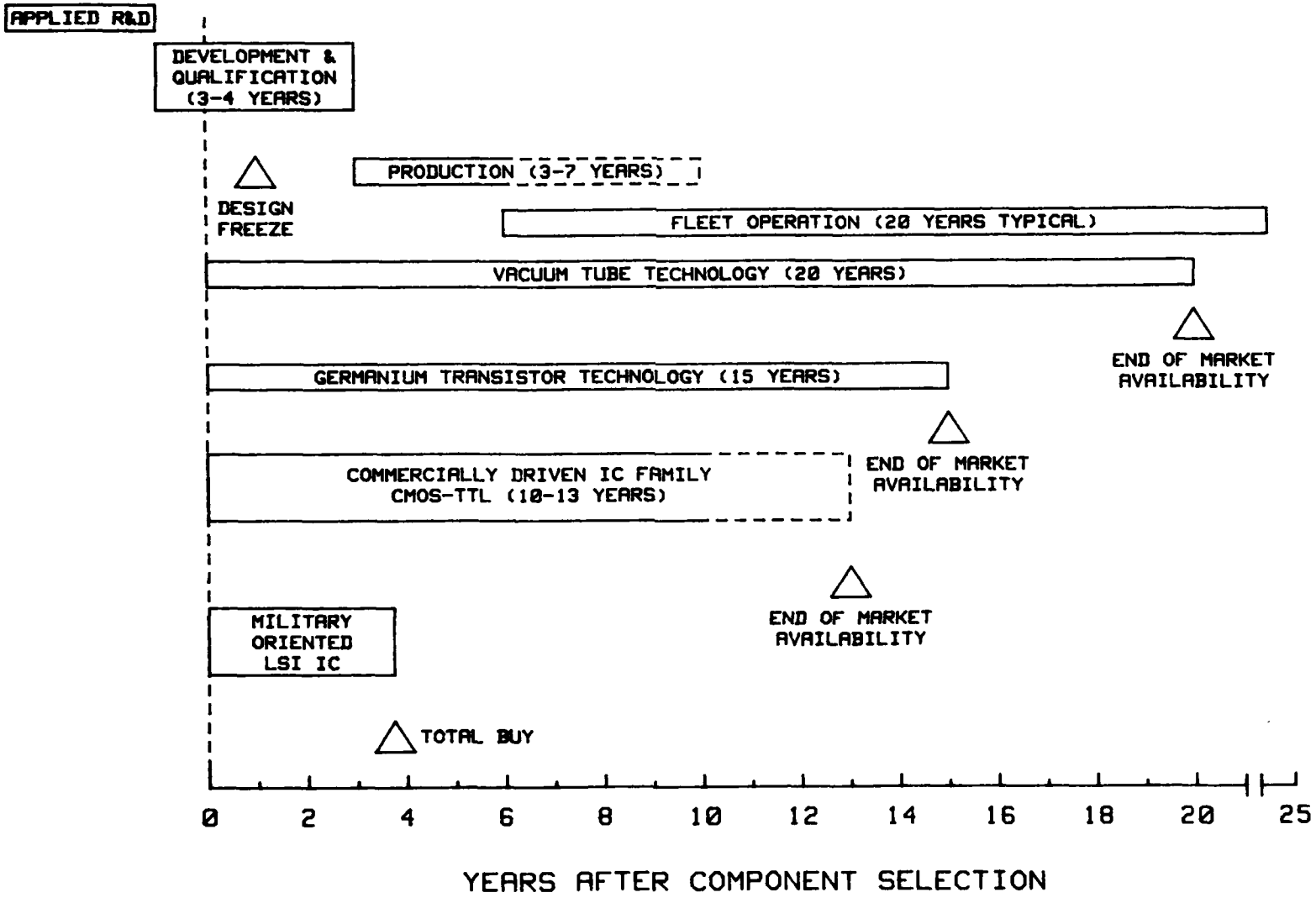


FIGURE 4-7

lifelong support of advanced microcircuit technologies and devices in avionics and related equipments. At the present time, management plans are being developed and set in operation for configuration-controlled development, acquisition, utilization, and support of those NAVAIR equipments implemented in commercially-driven IC technologies.

The elements of the program include: (a) application guidance and control to facilitate timely and controlled application of advanced microcircuit technologies in avionics designs; (b) timely visibility as to the life cycles of microcircuit technologies/devices utilized in avionics such that an "early warning" of pending obsolescence can be provided; (c) assessment of the impact on affected equipments and platforms; and (d) evaluations of corrective actions needed to maintain avionics systems in an operational status.

A major element of the COMPRESS program, the Impact of Microcircuit Part obsolescence on Avionic Critical Technology (IMPACT) system, was established to develop and place into operation semiconductor technology monitoring and data management techniques whereby early warning of pending part obsolescence and their impact on NAVAIR equipments can be assessed. This system is an integration of semiconductor market visibility procedures, data base management techniques, and microcircuit data collection, which is being structured to provide answers to four basic questions concerning disappearing microcircuits and technologies utilized in NAVAIR equipments:

* What microcircuits/technologies are obsolete or are in danger of becoming obsolete?

* What obsolete microcircuits/technologies are used in NAVAIR equipments?

* In what assemblies and how many times are the obsolete microcircuits/technologies used?

* What corrective actions should be taken? By whom? And when?

The IMPACT system is supplying NAVAIR acquisition managers and logistic support personnel with pertinent information regarding the location of obsolete microcircuits within the platform of interest, down to the equipment assembly level. The concept of procuring microcircuits on a contingency basis in wafer or die form (lowest cost) during the time they are being manufactured and then storing them for possible future packaging and testing, as necessary for logistic or mobilization needs, shows promise to ease the problem of the impact of discontinued microcircuits on the operational status of avionics and related equipments. The function of acquiring, storing and providing these contingency microcircuits for utilization in affected equipments is also being considered by the COMPRESS program.

4.2.3 Summary

In summary, it must be realized that almost all devices derived from electronic technologies, will, after a period of time, become obsoleted by improved, more efficient devices spawned from still newer technologies. The rate at which technologies and resultant component products become obsolete will continue to be accelerated as semiconductor design, production, and test

facilities are improved to meet the volatile, competitive consumer product market. This accelerated volatility will impact acquisition, operational availability, and logistics support of avionics equipment via unavailability of components for production and repair parts, high redesign and requalification costs of replacement components/modules/subsystems, production and logistics delays, and general lack of system availability. If future acquisitions of new aircraft and associated electronic equipments are to gain the advantages offered by the advancing volatile commercially driven electronic technologies, the associated constraints must first be minimized. Decreased economic incentives, long design times and high costs, rapid device obsolescence, and basic dichotomies between the nature of revolutionary electronic technologies and fundamental military procurement, deployment, and support procedures are creating critical Navy problems which must be addressed and resolved. If solutions to these complex problems are not formulated and corrective actions properly implemented, the end result of uncontrolled advanced technology application in Navy equipments will severely degrade fleet operational readiness.

4.3 SOFTWARE

Modern tactical weapon systems make extensive use of embedded computer software to perform many combat related functions. Not only are more and more systems and equipments using computers, or processing hardware elements, but the complexity of computer programs within this hardware is expanding radically.

Attempts are currently being made to reduce the cost of software development and maintenance through the use of automated aids. These tools cover software requirement specification, software development, and software maintenance. Software Requirements Engineering Methodology (SREM) and Software Design and Documentation Language (SDDL) are two examples of automated aids for the specification of software requirements. Automated facilities for the production, validation, and maintenance of military, real-time software are currently in use. All of these tools are intended for use with high-level, structured languages.

Problems with these tools exist, however, impairing their usefulness and cost effectiveness. Primarily, the tools are limited to the specification and production of software for a single, centralized computer, and do not have the capability to handle multiple computer systems, especially in those cases in which the computers have different instruction set architectures. More development is required in this area.

A secondary problem is that most high level languages have no capability to handle Input/Output or control of concurrent processes, especially in the non-standard, time-critical world of Naval avionics systems. The new standard language ADA attempts to address this problem.

In the area of software management and documentation, the Navy has mandated strict adherence to a number of military standards (e.g., MIL-STD-1679), TADSTANDS, DoD directives, and NAVAIRSYSCOM instructions. As these documents are applied and software management principles become more disciplined, the problems associated with software will gradually diminish,

although software and software support will continue to be a problem well into the decade. Considerable progress has already been made, as evidenced by the development of both hardware and software standards. Strict adherence to the requirements of planning documents, DoD directives, TADSTANDS and NAVAIRSYSCOM instructions will be required to fully bring software management under control. The following sections describe the significant software support issues and major software support activities that have been established.

4.3.1 SOFTWARE SUPPORT ISSUES

4.3.1.1 Background

Avionics software is one of the most complex elements of an avionics system. This complexity is due to the wide range of computational and control functions performed by the system computer, each step of which must be defined in extremely fine detail by the software. The complexity is increased by the fact that the dynamic, operating form of the software is not the same as the static form evidenced by program listings or card decks. Internal decisions based on computational results, the end of certain time intervals, or interrupts caused by system events can cause execution sequences which are difficult to predict deterministically from program documentation. The avionics software defines and provides many of the functional capabilities of the system and its sensors. It acts as a central integrating element for the system, providing control and computation functions which often give the system greater capabilities than would be found in its individual parts. Finally, the software provides an interface to the operator, tailoring system characteristics to the information and control requirements of human operators.

Outside the confines of the aircraft avionics system, software is increasingly becoming a part of the stores and weapons attached to the aircraft which exchange information with the avionics equipment. Further outside the aircraft system, but intimately associated with it, is the software found in both peculiar ground support test equipment, and in various trainers.

Also associated with the avionics software is the array of support software, such as assemblers, compilers, and simulators required for the development and support of the avionics software.

The development of high-quality, complex software requires skilled personnel, access to significant computational power (e.g. computers that host and execute support software; microprocessor support/development systems), and extensive support software, and adherence to comprehensive documentation disciplines.

The design, development, testing and life cycle support of this array of software has become a cost component that is typically large with respect to the cost of the computer and its peripherals and interface equipment.

4.3.1.2 Current Status

Software technology is now very much in a state of dynamic transition. Many products of past inadequate practices in software design, documentation, and test remain deployed in large numbers of weapon systems in

the Fleet. On the other hand, newer computer controlled weapon systems are being developed which embody some of the most modern concepts of software development, documentation and support.

There are approximately 14 unique avionics computers deployed in Navy aircraft. Each of these provides highly centralized computation, decision making, and control for navigation, weapons control, and/or a variety of other mission control functions. Except for the family of standard Navy computers that emulate the AN/UYK-20 [this includes the AN/AYK-14(V)], each of these computers uses software that was designed using a unique language and a unique support software package. Generally, a unique program loader/verifier equipment is required. The training and experience of programmers and software support personnel on one computer cannot be easily applied to other computers because the training and experience tend to be unique to each computer type.

A variety of microprocessors and microcomputers is finding its way into avionic equipment. In at least one case, the vendor has taken the attitude that the operational flight software (OFS) for these computers, which is frequently stored in a read only memory (ROM), is not a software item. The ROM is considered to be hardware which is "manufactured" by loading the OFS. In keeping with this attitude, the software is frequently not documented to the extent to which other knowledgable, professional programmers could quickly learn the software and be able to modify and/or support it. The Navy may not even own the documentation that does exist. This situation cannot be allowed to be repeated in other systems.

Many of the operational and support digital computer programs that have been developed in the past are not modular; they are a single unit. This makes modification and support very difficult because variable names and computation steps must be changed throughout the entire program.

4.3.1.3 Perceived Trends

The practice of procuring a new mission digital computer for every Navy aircraft type is gradually being brought under control by the requirement to use one of a family of Navy standard computers and one of a limited set of standard programming languages. From a logistic (hardware and software) support point of view, the use of standard computer hardware and software is an immensely powerful concept, if implemented quickly and decisively. At present, the state of availability of standard software languages is somewhat advanced with respect to the availability of standard hardware. The trend toward the use by the Department of Defense (DoD) of standardized computer hardware and a small family of highly developed, well documented programming languages will continue throughout the next decade.

The development and improvement of automated aids for the specification and maintenance of software will continue.

The employment of microprocessors and microcomputers and associated memory devices, programming languages and peripherals is an area of considerable disorder. For example, in one aircraft avionic system alone, there are 10 microprocessors/microcomputers of 6 different types. They are not all standard military qualified devices. Some do not have second sources. No

standard programming language is used, and the Navy does not presently have or own documentation of the programs executed by the microcomputers/ microprocessors. The systems prime contractor originally regarded memories containing OFS as "hardware" that was "manufactured" by loading the OFS. This is a logistically impractical concept.

The trend in microcomputer/microprocessor support includes several very powerful concepts and some very significant steps:

* A standard Navy microprocessor, the AN/UYK-44(V), is now in development. This will provide much needed standard computing hardware, which in turn, will reduce the number of unique microcomputers/microprocessors deployed and tend to control the now uncontrolled hardware logistic support burden and the problem of long term replacement parts availability.

* The AN/UYK-44(V) uses the same family of standard programming languages and standard support software as the AN/UYK-20 and its emulators.

* Programming generated for microcomputers/microprocessors will come to be regarded in the same manner as programming for minicomputers. The existing requirements for top down design and modular structure will be imposed. Existing documentation requirements will also be imposed.

The trend is now strongly away from the use of huge, monolithic, almost-unsupportable digital computer programs. Current requirements documents, such as MIL-STD-1679 Weapon System Software Development, support this trend, which will continue throughout the next decade.

4.3.1.4 Areas Requiring Further Development

Current - The entire concept of standardized hardware and operational and support software should be carried out in an aggressive and expeditious fashion.

* The refinement of the components of the standard family of Navy programming languages should continue.

* Development should begin on a family of interpreters to translate compiled ADA (the standard DoD programming language) programs into code executable on Navy inventory computers.

* The development of the AN/UYK-44(V) should be aggressively pursued.

* A small family of standard microcomputers and microprocessors, designed for tasks ranging from simple to complex, should be developed.

* The development/improvement of automated software production aids should be pursued, especially in the area of multicomputer system software support.

* The development of a unified concept of how software will be supported in the Navy should be initiated. This concept should ensure that the efforts of R&D manpower can be used to develop new weapon system concepts rather than be expended in the logistic support of existing systems.

Short Term (0 to 5 years) -

* Complete the development of the AN/UYK-44(V). Continue development of a small family of standard microcomputers/ microprocessors designed to handle tasks ranging from simple to complex.

* Continue the development of ADA interpreters/translators and improved automated software production aids.

* Complete the development of a unified concept of Navy software support.

* Continue refinement of software development and documentation facilities, development software, and software documentation.

* Continue development of languages that tend to be self documenting. Commence development of advanced languages which will dictate computer hardware development.

Mid Term (5 to 10 years) and Long Term (10 years plus) -

* Complete development of the small family of standard Navy microcomputers/microprocessors.

* Complete the development of ADA interpreters/translators.

* Implement the unified concept of Navy software support.

* Continue development of advanced languages which will result directly in the design of hardware tailored to that language.

4.3.1.5 Development Priorities

* The development of ADA interpreters/translators should be given a high priority, along with development of tools to produce ADA software.

* The second priority item should be the continued rapid development of the AN/UYK-44(V) and a small family of follow-on microcomputers/microprocessors.

* The development of a unified concept of Navy software support, consistent with other Navy logistic concepts, should also be commenced.

4.3.1.6 Summary

There is an abundant supply of excellent documentation governing software development and support. These documents consist of military standards, TADSTANDS, software management manuals, NAVAIRSYSCOM instructions, background and planning documents, etc. Standardized computer hardware and software families are now well along in development. Some of the major areas of future progress should be as follows:

* It must be clearly recognized that software support is a major and legitimate cost element in avionic system development.

* Top level management attention must be given to the development, documentation, and long term support of software.

* High priority must be given to providing adequate funding for on-going software support activities and the development of new, advanced software support tools.

Some useful software tools would be:

(a) Documentors, which would generate data base design documents and program description documents directly from source codes.

(b) Test analyzer, which would assist in ensuring that software tests are reasonably exhaustive.

(c) A file management system, to facilitate the tracking of code development.

(d) A PDL analyzer, utilizing a Program Design Language (PDL) based on Ada.

Some of these tools are already in existance and see limited usage in isolated areas. Two things are needed to make them of benefit to the Navy:

(a) Availability

(b) Training

First, they need to be available throughout the Navy. This could be accomplished by integrating the software tools with the MTASS package. Some of this is already being done with the MTASS/L development. Second, software developers need to be aware of their existance, and be familiar enough with their operation to be confidant in their use. This could be accomplished by means of a Navy - wide training program. Such a training program should also include software development management and modern design and coding techniques. This would greatly improve the Navy software development process. Such a course could be given to both Navy and contractor personnel.

A unified concept of Navy software support is also needed to ensure that the logistic function of long term software support does not degrade the capability of the Navy R&D community to develop new weapon system concepts.

4.3.2 SOFTWARE SUPPORT ACTIVITIES

4.3.2.1 Background

NAVAIR has established at various sites the peculiar integration and simulation facilities necessary to support the tactical support software for the individual Weapons Replaceable Assemblies (WRA's) and the total individual aircraft weapons systems. Software maintenance and configuration control are large and legitimate cost components of the total weapons system support. A budget line item under Operations & Maintenance, Navy (O&M,N) has been established to maintain the total aircraft weapons systems throughout the life cycle of the equipment.

4.3.2.2 Current Status

Software support (maintenance) is now being performed by several Navy laboratories and centers who function as software support activities (SSA's). The weapons systems which are currently being supported or which are planned for the near future and the Navy SSA assignments are listed as follows (on following page).

4.3.2.3 Perceived Trends

The funding requirements of the O&M,N software budget have grown at a rapid rate due to the introduction of new, complex, software intensive aircraft weapons systems. It is anticipated that the requirements for O&M,N funds will continue to increase as newer systems become operational and older systems, upgraded with new minimum requirements, require continued support.

It should be noted that O&M,N funding requirements estimated by the individual SSA's now exceed the available funds by 50 to 75%.

Software Support Activity Assignments

WEAPON SYSTEM/EQUIPMENT	NAC	NWC	NADC	PMTC	OTHER
A4M		X			
A6E		X			
A7E		X			
AIM-7M		X			
AV-8B		X			
AWG-21		X			
AYK-14	X				
CAINS	X				
E-2C					X
EA6B				X	
EP-3E					X
EWSSA				X	
F-14				X	
F-18		X			
HARM		X			
LAMPS			X		
P-3B					X
P-3C			X		
S-3			X		

4.3.2.4 Areas Requiring Further Development

The areas associated with SSA operation and the expenditure of O & M, N funds which require further development include:

* More precise definition of minimum sustaining funding levels for the individual SSA's.

* Better accounting of software maintenance effectiveness, i.e: number and classification of software deficiencies corrected versus O&M,N dollars expended.

* Development of long term plans to satisfy funding requirements for the maintenance of weapons system software.

* Development of a long term plan to achieve maximum economies in the maintenance of weapons system software including an investigation into the feasibility of establishing a single field activity site for software support.

4.3.2.5 Development Priorities

The most immediate priorities are the development of more precise definitions of minimum sustaining funding levels for the individual SSA's and better accounting of software maintenance effectiveness. NAVAIR has developed a plan to audit the individual SSA's during FY 81. The data resulting from the audits will be utilized to define minimum sustaining funding levels and software maintenance effectiveness.

4.3.2.6 Ongoing Programs

See Figure 4-8.

4.3.2.7 Summary

Software support activities play a very active and important role in maintaining Fleet tactical support software for aircraft weapons systems. The importance of this role will increase as Fleet weapons systems become increasingly software dependent. Action is required to ensure maximum effectiveness in the operation of the SSA's.

4.3.3 AVIONICS SOFTWARE LIFE CYCLE MANAGEMENT AND COSTING

4.3.3.1 Background

To meet current and future threats, albeit within severe budgetary constraints, the growth in the sophistication and complexity of avionics systems has accelerated rapidly in recent years. Accompanying this increased complexity has been an increase in software required to support the execution of the required missions with a high probability of success. Recent trends have shown that the cost of acquiring and supporting software has risen relative to the cost of avionics hardware on which the software operates. In fact, it has risen to the point that software is currently a significant percentage of the total cost of most major avionics system projects. The

MAJOR MILESTONES FOR SOFTWARE SUPPORT ACTIVITY

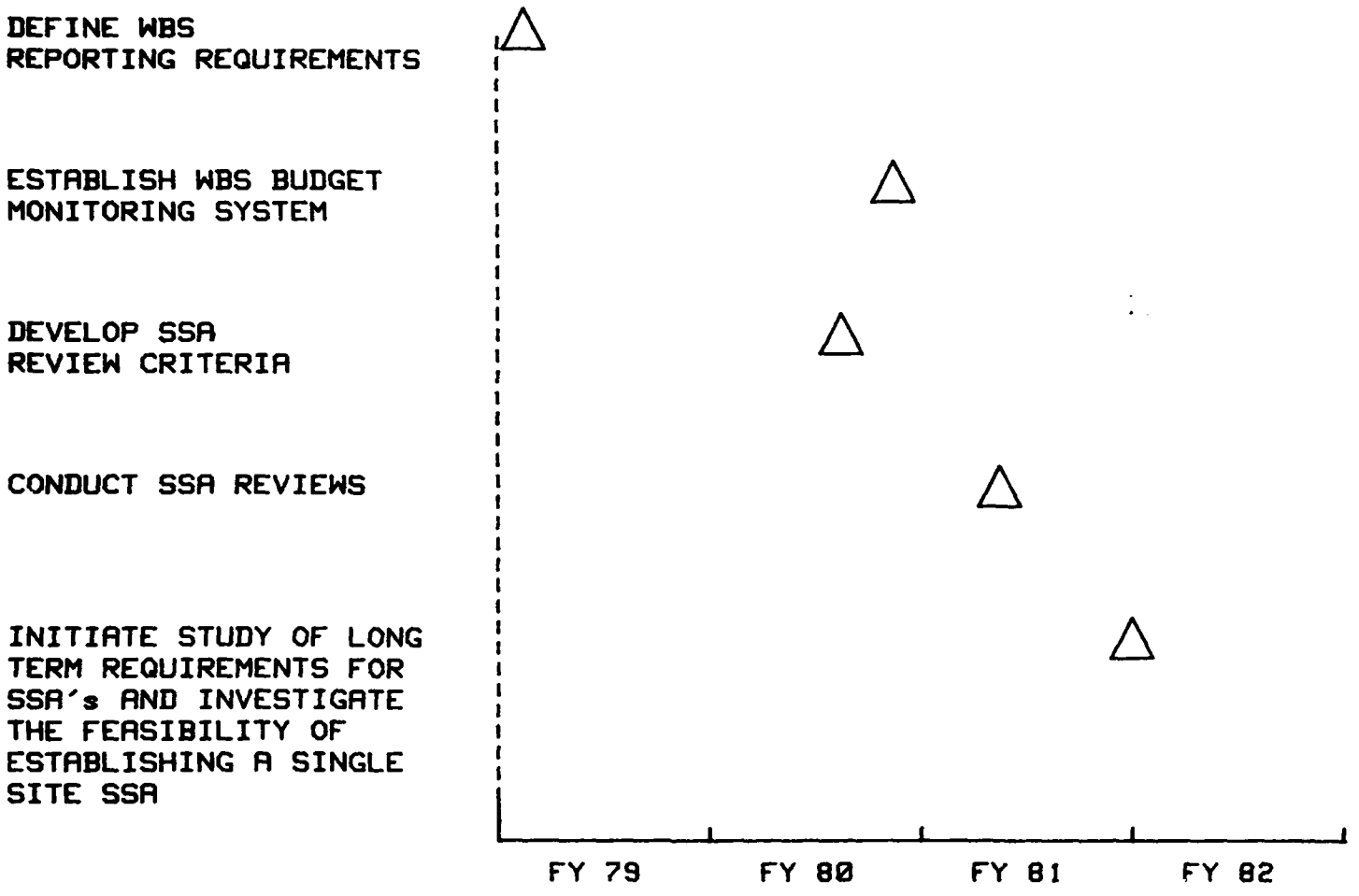


FIGURE 4-8

development and application of software management control techniques, including cost estimating methodology, has not kept pace with the emergence of software as a significant development product, and software maintenance as a significant operating and support activity. Given this state of affairs, it is a matter of necessity that the avionics community emphasize an enhancement of the quality of the methodology used to manage and estimate the life cycle cost (LCC) of the software elements of a total avionics system.

4.3.3.2 Current Status

The Naval Air Systems Command is intensely concerned with software costs of major naval aircraft and avionics system programs. Recognizing this concern, an Independent Exploratory Development (IED) effort has been established to enhance the Navy's capability to estimate software costs at various stages of the acquisition cycle. The objective of this IED program is to investigate the adaption of existing methods to estimate the life cycle cost of software programs/systems including design, implementation, test and integration, verification and validation, and maintenance/updates.

4.3.3.3 Perceived Trends

There will be significant attempts within the Department of Defense and among the services to standardize, or develop standards for the cost of developing software with special attention devoted to the collection of cost data. The Naval avionics community is not well prepared to participate in this process, and is not working at the cutting edge of the state-of-the-art in these disciplines. This requires an urgent assessment of the situation and the development of plans to remedy it.

4.3.3.4 Areas Requiring Further Development

Current and Short Term (0 to 5 years) -

* Develop a uniform methodology for collecting software management and cost data for avionics programs. Pertinent data would include software development manpower, program sizes, schedules and cost.

* Develop a statistical data base of completed avionics software programs to assist in the derivation of cost estimating relationships.

* Acquire proven estimation models (commercial and inter-service) for estimating costs of avionics software and adapt the models for Navy use.

* Develop software sizing and cost models based on historical data. Develop criteria for estimating the uncertainty in size and cost projections.

* Establish criteria and techniques for deriving a software sizing capability and attendant program development costs for avionics programs under varying assumptions of program development constraints.

* Develop methodology for tracking software costs for ongoing projects, and for correcting estimates because of program changes and ECP's.

Mid Term (5 to 10 years) and Long Term (10 years plus) -

* Compile a software cost estimating guide for use by avionics software development managers and cost analysts, for their use in deriving cost estimates during the early stages of systems acquisition.

* Contibute to the avionics software development community by advancing the state-of-the-art in cost data collection and cost estimation modeling techniques.

* Develop software cost estimation tutorials for use throughout the Naval aviation community.

* Advance the state-of-the-art to the point whereby the Navy would be a recognized leader among the Services (Army, Navy, Air Force) in the management of software development and in software cost estimation.

4.3.3.5 Development Priorities

The primary emphasis should be on the urgency of development of a uniform and agreed upon method for collecting Navy avionics development program data to identify those which should use existing software costing techniques. As soon as this is accomplished start a training program to acquaint the program developers with the existing techniques and adapt these for their use. Beyond that, advancing the current (not yet entirely satisfactory) techniques becomes the priority issue.

4.3.3.6 Summary

The relevant priority issues are:

* Data collection and uniformity for use of current techniques,

* Advancement of current, not entirely satisfactory, techniques, and

* Facilitate the use of proven management practices to enhance development productivity and reduce the cost of software development.

4.4 ARCHITECTURAL TRENDS

Avionic systems in the 1990s and beyond will be radically different than the preponderance of those in the Fleet today. To support the long range requirements of multi-mode, multi-mission aircraft anticipated for future naval operations, the very nature of systems architecture must change. The use of new technologies will be required to yield the necessary operational sophistication to avoid generation of incredibly expensive and complex hard-

ware configurations. System unique, point-to-point wiring and cabling will be replaced by multiplexed video and signal digital data buses, allowing high speed transfer of data and the use of common connections to all boxes in a given avionics network. Large, centralized computers will be replaced by or augmented with numerous embedded microcomputers and/or microprocessors, capable of significant processing within the local circuitry before entering a digital data bus array for distribution. Auto-diagnostic capabilities will increase significantly. These capabilities will allow prompt repair and/or replacement actions at the operational sites. These increased auto-diagnostic capabilities, including those of multi-level auto-diagnostic analysis, will provide the basis for highly effective auto-reconfigurable weapons systems that are capable of recognizing failures in the original system configuration and reconfiguring the system to insure that the maximum number of highest priority functions continue to be performed throughout the mission. Systems will tend to be more and more dependent upon distributed processing in non-dedicated portions of the system matrix. Subsystem boundaries will become less physically identifiable because they will be functional in nature. A higher degree of interaction will result, with constant or potential dependence upon parts of seemingly unrelated systems. Processed, high level data will be shared system-wide through the use of multifunction, multilevel, auto-reconfigurable digital data buses.

Distributed processing is considered a development area in which the move is away from large, complex central processor architecture with its complicated software and input/output (I/O) hardware to smaller, locally-distributed processors. Many benefits can accrue from this type of distributed architecture, such as system auto-reconfigurability, graceful degradation, lower cost for hardware and software, higher "mission" reliability, and better fault isolation for both hardware and software. The more powerful distributed processing systems will be capable of dynamic allocation of processing resources in an optimal fashion to provide maximum utilization of the resources and yield the highest instantaneous mission performance capability. Efforts must be concentrated on development of fault isolation and reconfiguration techniques, system design and evaluation tools, and utilization of advanced technology developments such as fiber optics and Very High Speed Integrated Circuits (VHSIC).

Standardization is also a very important issue when advanced architecture is considered. The different functional blocks in any type of distributed system must interface with the rest of the system in a "standardized" manner to permit ease (and affordability) of integration, multiple platform utilization, reconfiguration, and a reduction in the proliferation of interface/bus definitions and Peculiar Ground Support Equipment. Standard data buses, such as the serial, time division multiplex data bus defined by MIL-STD-1553B, are gaining wider acceptance and are being applied in major Navy avionic systems such as LAMPS MK III, F/A-18, and AV-8B, as well as uses in Air Force and Army equipment. Development efforts are in process for wide band data buses and a fiber optics MIL-STD-1553 compatible bus.

An advanced, modular, functionally integrated approach to communication, command, control, navigation, and identification (C^3NI) system architecture under development is the Tactical Information Exchange System (TIES). Programmable systems hardware is employed by this concept at the

functional module level (i.e., IF strip, receiver front end, etc.) Alternate routing of signals through appropriately programmed functional assemblies is provided by a multiple level bus structure. Many of the benefits that are characteristic of distributed processing also accrue to the TIES architecture such as an estimated 40 percent reduction in size and weight over "Black Box" architecture and the ability for graceful degradation, never totally losing a significant function (i.e., IFF, ACLS, Voice, etc.). Such a concept could also be expanded to include functions other than C^3NI and offers significant promise for ushering in totally integrated avionics systems in the 1990s.

Each of the architectural developments and trends highlighted in this section are considered essential to transition from current avionic architecture to the highly integrated, auto-reconfigurable, reliable, and capable architecture necessary in the 1990s.

4.4.1 DISTRIBUTED PROCESSING

4.4.1.1 Background

The use of large single processor machines in avionics has resulted in complicated software with inherent software reliability concerns. The advent of inexpensive microprocessors makes possible the implementation of a distributed processing system which may offer life cycle cost advantages over a single high-speed processor and allow for more built-in checks on both hardware and software malfunctions. Distributed processing consists of multiple processing resource components that can be assigned/reassigned to specific tasks on a dynamic basis in order to complete a required operation.

The use of distributed processing can also enhance the capability of avionic systems to degrade gracefully instead of catastrophically. Decentralized control can increase the flexibility and reliability of avionic systems. If the avionic system components are distributed physically as well as functionally, the survivability of an aircraft subject to battle damage is substantially increased. Lower cost, higher performance, and the greater reliability of distributed processing versus centralized processing will promote its use in avionic systems.

Distributed processing will also require more complete partitioning and definition of avionics functions than has previously been necessary. This partitioning, coupled with well defined, standardized system interfaces and protocols, should decrease the cost of modifications and greatly enhance system flexibility and expandability.

4.4.1.2 Current Status

While the concept of distributed computation has the potential of greatly enhancing the capability and survivability of military aircraft, there are practical and theoretical problems which must be addressed.

Present system design procedures are not capable of producing an optimal allocation of functions to processors for large distributed systems, especially when qualitative requirements such as fault-tolerance and flexibility are imposed.

Present serial data bus structures do not have sufficient speed (bandwidth) to allow processor-to-memory communication in a distributed system. The need for additional protocol and error checking compound this problem. Lack of a wide bandwidth data bus has resulted in the selection of architectures minimizing inter-processor communication. Major processing blocks have been centralized in a single processor which precludes reconfiguration upon subsystem failure.

Currently, the behavior of software programs in a distributed environment is not adequately understood, especially in the event of a component failure. While sound reassignment and partitioning strategies appear to exist for the special case of structured software design, practical implementation of such strategies in an avionic application is yet to be accomplished.

Tools for the evaluation of distributed systems are presently inadequate. While both stochastic and analytic simulators for distributed systems exist (or are under development), most are inadequate, difficult to use and cannot be employed at multiple levels of detail.

4.4.1.3 Perceived Trends

There is an increasing awareness that system and intersystem data buses are prominent failure prone elements. Various inter-processor bus schemes are being evaluated to determine their susceptibility to undetectable faults and to test the capability of the bus structure to tolerate and repair.

The cooperative efforts of a number of small processors can outperform a large machine in many applications. New concepts in computer architecture are gaining acceptance, including data flow machines and computation network machines. Single instruction multiple data (SIMD) stream configurations are under development for signal processing applications, while multiple instruction multiple data (MIMD) configurations are considered best for data processing and control applications.

Unlike past processor developments, the design of a distributed processor system will be influenced by techniques needed to fault isolate the hardware and even more importantly to determine the effectiveness of the software.

Future data buses using fiber optics will provide sufficient bandwidth to allow processor-to-memory communication for distributed systems. Extensive inter-processor communication will be possible, which will allow rapid reconfiguration and graceful degradation upon subsystem failure.

A compiler for a distributed system differs significantly from compiler designs for single processor systems. Two approaches are being considered. The first technique would use a highly sophisticated compiler that would a priori address such tasks as processor assignment/reassignment, single and distributed resource management, and hetergeneous instruction sets. The second technique under investigation would use simple compilers minimizing configuration specific information; hardware-assisted operating systems would be used for designating distributed processor assignments.

Layered protocol approaches presently being developed in the data communications community will influence standard system interfaces in avionic equipment. These interfaces include operator-to-system, application program-to-application program, application program-to-hardware driver, executive-to-local executive and hardware-to-hardware interface.

Developments resulting from the Very High Speed Integrated Circuits (VHSIC) Program will prove useful to distributed systems in the implementation of fault tolerant bus schemes, high speed system control functions and special purpose signal processing functions. The historical trend towards faster, smaller, and less expensive computers will be extended and accelerated.

New memory organizations will be developed which will marry physically separated memory to high-speed, serial, data bus structures. These will minimize memory contention between processors while maximizing concurrent operation. VHSIC implementations will increase the use of content addressable memories, and other "smart" memory configurations. Solid-state, bulk-storage, devices (NMOS, Bubble, CCD, etc) will replace current disk, drum and tape implementations.

4.4.1.4 Areas Requiring Further Development

Current -

* Development of design methodologies and partitioning algorithms for distributed systems.
* Use of MIL-STD-1553B to achieve a limited varient of distributed processing.
* Development of a high-speed fiber optic bus.
* Development of distributed system simulators and other evaluation tools.
* Design of microprocessors with emphasis on software and higher-order-languages.

Short Term (0 to 5 years) -

* Development of high-speed, fault-tolerant serial and parallel bus structures.
* Implementation of common high-speed processing functions in VHSIC.
* Development of system interface standards.
* Development of automated distributed system design and evaluation tools.
* Development of fault isolation and reconfiguration techniques.

Mid Term (5 to 10 years) -

* Development of specialized processors for distributed systems.

* Implementation of distributed systems using standard computers and buses in new platforms or a major CILOP to an existing platform.

* Development of applicable VHSIC devices.

Long Term (10 years plus) -

* Development of very low power integrated circuits.

* Implementation of fully distributed systems using advanced VHSIC technology and high level language.

4.4.1.5 Development Priorities

* Fault-tolerant bus structures must be defined and hardware mechanizations of distributed processing configurations must be tested.

* System design and evaluation tools need to be developed.

* Intra-processor and inter-processor interface standards must be developed and tested with simulators using real-world applications.

* Embedded self-monitoring tools must be developed to facilitate the analysis of the various proposed types of distributed systems and to aid in selecting the most promising technique. Self-diagnosis methods will have to be developed concurrently with hardware to determine the effectiveness of the system's fault tolerance.

* Special test programs must be developed to assist in the analysis of distributed systems and reflect the specific needs of a distributed avionics system.

4.4.1.6 Summary

The advent of inexpensive computational hardware has made the concept of distributed computing both feasible and attractive, because of the potential for improved fault-tolerance, flexibility, and performance. Many efforts to realize this potential are currently being pursued, including development of partitioning algorithms, definition of interface standards, and development of evaluation tools. Additionally, technology efforts include development of high speed buses, VHSIC, and other than present day Von Neuman type processing machines. High level languages for distributed processing are being developed.

In order to realize the potential of distributed processing for Naval avionics, system interface standards must be defined, design and evaluation tools must be developed, and VHSIC technology must be exploited. Fault-tolerance and flexibility must be designed into these systems, rather than calculated after the design is complete.

4.4.2 STANDARD DATA BUS APPLICATIONS

4.4.2.1 Background

Avionics integration, which can be defined as the cooperative use of shared information among avionic subsystems, became a necessity when operational requirements precluded the use of air vehicles with independent and self-sufficient subsystems. Subsystems were forced to depend on each other for information. This level of integration began with complex subsystems which had the greatest information requirements. As digital technology progressed, this central subsystem took on other tasks not specifically related to that particular subsystem or to a display. Problems surfaced early in this central processor approach because the subsystems were designed with no concern for the connections to other subsystems. As a result, each of the interfaces with the subsystems reflected the specialized nature of the subsystem. Therefore, the input/output (I/O) portions of these central processors were large compared to the actual processing circuitry. Some of the problems encountered in centralized processor architectures were with the large complex I/Os. It was reasoned that these problems could be alleviated by partitioning and distributing the I/O circuitry. The use of multiplexing was fostered on aircraft because information transfers were convenient and the I/O was simplified and distributed. The aircraft wiring volume and weight were also significantly reduced.

With the development of smaller and more powerful minicomputers and microcomputers, some of the central processing functions were being distributed to other subsystems as well as the I/Os. Also, the multiple computer architectures added a desirable characteristic of redundancy.

Both hardware and software are affected when integration is implemented using multiplexing. Information transfer formats and electrical interface characteristics must be defined. Attempts at standardizing on a time-division multiplex serial data bus began with the Society of Automotive Engineers (SAE) establishing a subcommittee, Multiplexing for Aircraft (SAE/A-2K), in 1968 to define basic requirements of a serial data bus. The first version of MIL-STD-1553 was adopted in 1973. After extensive review and several revisions by the Navy, Air Force, Army and private industry, the MIL-STD-1553A version was approved in 1975 as a Tri-Service Standard. Since that time, industry and the military have continued to coordinate the Standard through studies, symposia, and development programs. With the availability of MIL-STD-1553A, industry and the military began to apply it, which surfaced some additional problems. Again, a revision (MIL-STD-1553B) was prepared as a cooperative effort and approved by the SAE/A-2K and the military in 1978. MIL-STD-1553B is a Tri-Service Standard and has been adopted by NATO as well as the United Kingdom and Federal Republic of Germany.

4.4.2.2 Current Status

Three Navy weapon systems which use MIL-STD-1553 are currently under development: F/A-18, LAMPS MK-III and AV-8B. While several pieces of GFE are common between them, each of these systems utilize a different architecture, and thus some incompatibilities exist between the systems. A brief description of each weapons system follows.

F/A-18. The F/A-18 utilizes a dual mission computer architecture. Each of these processors is assigned a specific function, but can also assume the critical tasks of the other processor in the event of a failure. Both processors are interfaced to the remainder of the avionics systems by two dual standby redundant MIL-STD-1553 data buses. The data buses on the F/A-18 are controlled by a contractor specification which requires more stringent electrical characteristics for the data bus than those imposed by MIL-STD-1553. This additional specification limits the use by the F/A-18 of equipment developed for other programs.

LAMPS MK-III. The LAMPS MK-III uses two computers which communicate over a non-redundant MIL-STD-1553 data bus. Neither computer has the capability to assume any processing tasks from the other computer in the event of a computer failure. A second dual standby redundant data bus system provides a program load capability; however, this data bus system is not used for data transfers during system operation. Most of the terminals developed for use on LAMPS MK-III are not compatible with other avionics systems due to the lack of redundancy.

AV-8B. The AV-8B uses a single mission computer to accomplish system level data processing. A dual standby redundant MIL-STD-1553 data bus system is used to interface the mission computer to the remainder of the avionic subsystems. The data bus on the AV-8B is controlled by a contractor specification similar to the F/A-18 specification. The AV-8B mechanization thus is potentially incompatible with other MIL-STD-1553 equipments.

Numerous existing weapon systems, including F-14A, E-2C, EA-6B and P-3C, are scheduled to undergo engineering changes which will incorporate MIL-STD-1553 data bus equipments into the avionics systems. While most data bus equipment designed prior to 1980 met the requirements of MIL-STD-1553A, these updated weapon systems will use a combination of existing MIL-STD-1553A data bus equipments and newly designed MIL-STD-1553B equipments.

Several weapon system programs which will use MIL-STD-1553 data buses are currently in initial development phases. These include ECX, VTS, and VCX. While it is expected that these systems will use MIL-STD-1553B data bus systems, some MIL-STD-1553A equipments may still be used.

To support these weapon system developments, several programs are underway to develop data bus equipments which can be provided as GFE to the major weapon system developments and upgrades. The AN/AYK-14 computer currently provides a dual standby redundant MIL-STD-1553A interface channel. The design of a dual standby redundant MIL-STD-1553B channel is underway, and the new channels should be available during FY 82. The AN/ARC-182 communications transceiver is currently in final stages of engineering development. The control interface is a MIL-STD-1553B interface which has been designed to

be compatible to the maximum extent possible with the F/A-18 and the AV-8B. The Carrier Aircraft Inertial Navigation System (CAINS) program has developed the CAINS IA which uses a MIL-STD-1553A data bus compatible with the F/A-18 and the AV-8B. A new development, CAINS II, has been initiated which will retain the word formats of the CAINS IA but will meet all the requirements of MIL-STD-1553B. The Avionics Components and Subsystem (AVCS) program is currently developing several avionic equipments which will use data bus interfaces. The AVCS program will begin engineering development of a Digital Air Data Computer (DADC) during FY 81. This subsystem will use a dual standby redundant MIL-STD-1553B data bus interface.

4.4.2.3 Perceived Trends

The use of integration to improve the vehicle's mission performance has caused the vehicle avionics integrator to look at multiplexing as a method for achieving integration. In other words, the system design has become indistinguishable from the system design method. Also, there is great emphasis in the present military environment to extend the airframe life, thus causing the avionics system integrator to examine new approaches to avionic systems that will provide design flexibility to meet evolving missions and future threats. Integration using data buses is an important step in reaching these goals. The use of data buses, for example, allows the use of redundant subsystems for critical functions and the use of redundant information from various sensors, where available.

The Navy must establish the necessary controls to assure that the avionics architecture of new and upgraded weapon systems is designed to make use of the proper levels of redundancy. An effort must also be made to identify any GFE equipments which are appropriate for use in these weapons systems. Simultaneously, some newly developed equipments may be identified as future GFE.

Some recent Navy programs have identified a potential need for a data bus with a wider bandwidth than MIL-STD-1553B. Several advanced development efforts are currently underway which are evaluating data bus systems with data rates from 10 to 50 megabits per second. The SAE/A-2K committee has established a task group to review the requirements for a wide band data bus and to prepare a draft military standard. This effort will be completed in FY-82.

4.4.2.4 Areas Requiring Further Development

Current - To properly control the development of advanced avionics data bus architectures, the Navy will establish, under the Naval Air Systems Command, the function of Avionics Architect. The function of the Avionics Architect will be to:

* review proposed avionics systems architectures to optimize the configuration for flexibility, growth potential, and multiplatform use of subsystems and identify potential deficiencies,

* resolve incompatibilities between multiplex serial data bus implementations, i.e., MIL-STD-1553A, MIL-STD-1553B, and contractor specifications.

* recommend usage of available GFE where appropriate,

* identify subsystems which are candidates to become GFE,

* identify weaknesses in presently available technology and recommend advanced development programs to resolve problems,

To aid in these efforts, the Avionics Architect will adopt a standard data bus control specification to replace the various contractor developed specifications. This specification will be used to control all subsystem MIL-STD-1553 data bus interfaces. In this way, interoperability of equipments between weapon systems will be promoted.

To perform the necessary simulation, testing, validation, and advanced development, the Avionics Architect will use the available avionics simulation laboratories, including the NADC BASIC laboratory and the NAC DASL laboratory. These laboratories must continue to develop the necessary simulation software and interfaces to support these efforts. The laboratories must also begin investigations into wide band data bus architectures to support the development of the proposed wide band data bus military standard.

Short Term (0 to 5 years) - The primary emphasis during this time period must be the development of improved software techniques for the control of data buses. Foremost among the areas requiring investigations are dynamic bus control, degraded mode capabilities, and multiple sensor correlation.

Considerable effort must be placed in evaluating how a wide band data bus and a MIL-STD-1553 data bus system would interact on a weapon system. Along with this effort, the necessary software control procedures must be developed to optimize the functioning of the wide band data bus.

Fiber optic technology has been maturing at a rapid pace for several years. With the proper emphasis on engineering development, fiber optic technology will become a viable avionics technology during this time period.

Mid Term (5 to 10 years) - The technology developed for wide band data bus systems will be used to develop new equipments during this time period. Considerable effort must be spent developing the necessary avionics architectures needed for the proper integration of the wide band data bus. The increasing usage of fiber optic multiplex systems during this period requires the development of new network topologies, due to the interconnection constraints imposed by fiber optic coupling technology.

Long Term (10 years plus) - This period will be used to continue the evolution of fiber optic and wide band multiplex data bus technology. Analysis must be made at this time to determine if new multiplex technologies will be required for future weapon system architectures.

4.4.2.5 Development Priorities

The Avionics Architect function must be implemented at the earliest possible date. To support the efforts of the Avionics Architect, the avionics simulation laboratories, such as BASIC and DASL, must be rapidly augmented to

provide the necessary level of support. Efforts must be initiated to resolve software control deficiencies. Investigations must be initiated to support the development of a wide band multiplex data bus standard.

4.4.2.6 Summary

The rapidly rising cost of weapon systems requires that the Avionics Architect institute policies to ensure the maximum level of compatibility between systems and thus achieve a high level of interoperability of equipments between weapon systems.

4.4.3 MIL-STD-1553 FIBER OPTICS

4.4.3.1 Background

Use of the MIL-STD-1553 multiplexed digital data bus for integrating avionics subsystems is becoming widespread, implemented with twisted, shielded-pair wire. Fiber Optics (FO) technology has reached a level of maturity such that development of a MIL-STD-1553 compatible digital bus using FO transmission lines is feasible. Work is currently underway via programs sponsored both by NAVAIR and the Air Force Avionics Laboratory (AFAL).

Efforts conducted by the Society of Automotive Engineers (SAE) A2K Subcommittee task group are directed toward the preparation of a compatible MIL-STD-1553 standard applicable to fiber optics. While MIL-STD-1553 specifies a bipolar, three-level Manchester code, fiber optics systems using non-coherent light emitting diodes (LEDs) and high-speed photodiodes provide an optical Manchester signal that is unipolar. This presents certain difficulties for implementation of the invalid Manchester synchronization codes required by MIL-STD-1553, and places restrictions on circuit design. Although solutions exist to this interface problem, the least complex method of implementation would be accomplished by preparation of a modified version of the Military Standard that provides for a synchronization-bit coding scheme that is directly compatible with unipolar optical Manchester signals. Development of a practical FO MIL-STD-1553 data bus system requires that significant effort be expended to define system architectures compatible with both the physical layout of the candidate aircraft and constraints imposed by FO technology.

4.4.3.2 Current Status

Both the Navy and Air Force have developed MIL-STD-1553 compatible FO transmitter and receiver modules. The interface for these modules is defined at the logic interface of the Bus Interface Unit (BIU) chip prior to encoding. Data encoding from the unipolar optical Manchester code required for FO to the bi-polar, three level MIL-STD-1553 code is accomplished in the FO transmitter/receiver modules.

Preliminary work has begun on a conversion of the AN/AYK-14(V) Standard Airborne Computer to accept FO MIL-STD-1553 inputs, as required by the AV-8B program. The XN-2 chassis version of the AN/AYK-14(V) will be used for this conversion. The result of this effort will be a modified chassis and supporting documentation.

A modified version of the Military Standard for FO implementations of MIL-STD-1553 has been prepared for SAE-A2K Subcommittee approval, followed by a request for DOD approval. The FO Standard specifies the optical interface, but does not specify a standard implementation; any optical implementation that satisfies the data transfer requirements of MIL-STD-1553 would be acceptable.

4.4.3.3 Perceived Trends

An FO MIL-STD-1553 data bus will be used in situations where Electromagnetic Interference (EMI) problems limit the effective use of a twisted-shielded pair wire. EMI problems become increasingly important as the use of composite aircraft structures grows, since the shielding effect of the aluminum skin is lost. Initial applications of the FO bus will only address the standard 1 Mbps data rate. Evolution to higher speed versions ($\leq$ 5 Mbps) may follow as increased integration of avionic suites occurs.

As a totally integrated avionics suite is realized, with corresponding increase in the complexity of the avionics subsystems, MIL-STD-1553 buses will not be able to efficiently handle the data transfer needs. Wideband FO systems will be required to supplement or supplant the MIL-STD-1553 buses.

4.4.3.4 Areas Requiring Further Development

Current and Short Term (0 to 5 years) - An approved Military Specification for a MIL-STD-1553 FO bus is required before an FO multiplexed bus can be used in military systems.

The upgrading of the AN/AYK-14(V) Standard Airborne Computer to accept FO inputs must be completed, and FO interface modules for existing avionic subsystems must be developed to allow optical communications with the AN/AYK-14(V). In this time frame, the FO interface modules will be implemented as adapter modules added to existing hardware, though this is not an efficient or preferred approach.

Mid Term (5 to 10 years) and Long Term (10 years plus) - Investigation of methods for implementing optical data buses with data rates greater than the 1 Mbps rate of MIL-STD-1553. These will fill the data transmission requirement between the MIL-STD-1553 systems and the specialized wideband fiber optics data buses/links and be used in conjunction with MIL-STD-1553 data buses.

4.4.3.5 Development Priorities

The following priorities exist for FO MIL-STD-1553 development:

* Develop optical transmitter and receiver modules for an FO MIL-STD-1553 data bus.

* Develop reliable, low loss optical couplers (tee and star).

* Develop a family of militarized single fiber connectors (single channel, multi-channel, right/45° angle adapters).

AD-A097 522 NAVAL AIR SYSTEMS COMMAND WASHINGTON DC F/G 9/5
NAVAIR AVIONICS MASTER PLAN.(U)
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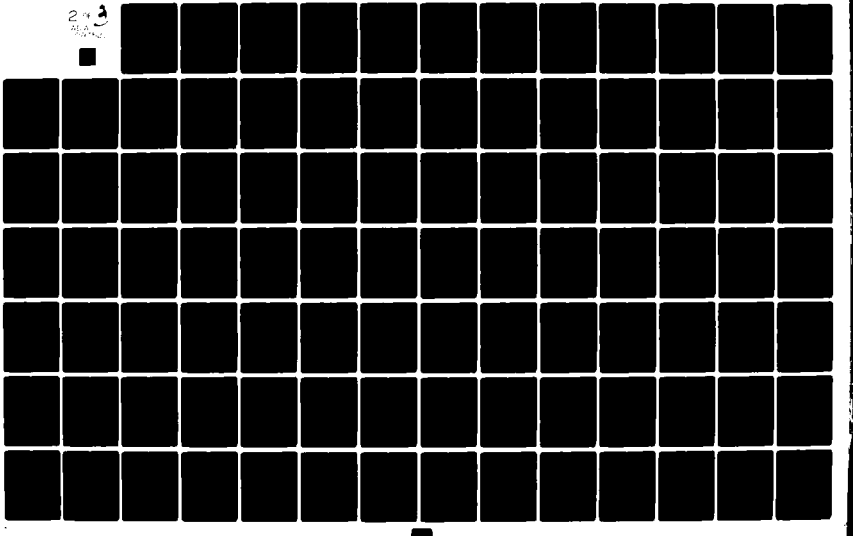

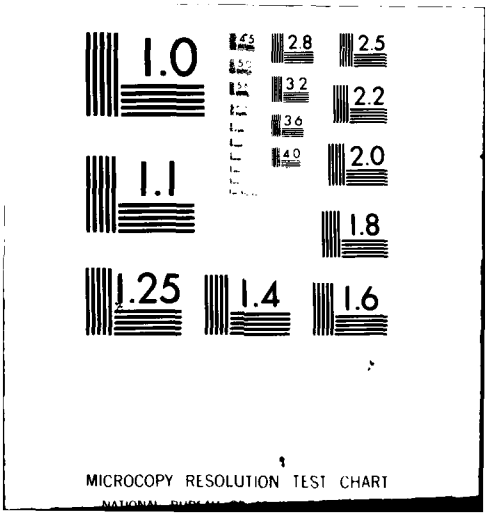
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MICROCOPY RESOLUTION TEST CHART

* Develop test methods for components and systems.

* Approve the FO Standard.

* Convert the AN/AYK-14(V) to MIL-STD-1553 (FO) compatability.

* Develop FO interface modules required to solve severe EMI problems in avionics subsystems.

4.4.3.6 Ongoing Programs

Currently an effort is being undertaken to investigate techniques to convert the AN/AYK-14(V) to MIL-STD-1553 (FO) compatability. Contingent on formal funding of this conversion effort, a 2-1/2 year effort would result in a modified chassis and support docuemntation.

4.4.3.7 Summary

An FO version of a MIL-STD-1553 data bus offers many advantages, especially if severe EMI problems exist and wide bandwidths are required. The EMI immunity will become increasingly important as the use of composite aircraft structures grows. Future avionics systems should be developed on the basis that an FO MIL-STD-1553 data bus will eventually be used on the aircraft for subsystem integration.

4.4.4 TACTICAL INFORMATION EXCHANGE SYSTEM (TIES)

4.4.4.1 Background

The growing sophistication in the naval air mission is especially challenging in terms of satisfying anticipated communication, command, control, navigation, and identification (C^3NI) requirements. Projecting into the 1990 timeframe, there will be an expected wide use of spread spectrum type communications in the Very High Frequency (VHF), Ultra High Frequency (UHF), and Lx bands; an advanced air traffic control system called Discrete Address Beacon System (DABS); a Global Positioning System (GPS) for establishing a very accurate geodetic position; Satellite Communications; and, Collision Avoidance. Existing functions such as amplitude modulation (AM) and frequency modulation (FM) voice, Tactical Air Navigation (TACAN), LINK 4, and LINK 11 must also be considered during the transition to newer, more advanced platforms. The proposed C^3 concepts, which are addressed in the C^3 subtask of the Sea Based Air Master Study Plan developed and promulgated by CNO, go much beyond the basic objectives of improving reliability and maintainability while reducing size, weight, and cost. There is an emphasis placed on higher level objectives including interoperability, adaptability, and forward/backward compatibility through distributed command and control with integration achieved through multiple tiered communication netting.

The Tactical Information Exchange System (TIES) approach is to develop a modular, functionally integrated advanced C^3NI system for air platforms to be introduced in the 1990-2000 timeframe. The concept employs programmable systems hardware at the functional module level (i.e., inter-

mediate frequency (IF) strip, receiver front end, etc.) and a multi-level bus structure which allows alternate routing of signals through appropriately programmed functional assemblies. The architecture results in an estimated 40 percent reduction in size and weight over "black box" architecture. Through the use of alternate path concepts and built-in-test (BIT), the overall system degrades gracefully, never totally losing any significant function (i.e., identify friend or foe (IFF), aircraft carrier landing system (ACLS), VOICE, etc.), thus resulting in improved mission reliability. The new systems architecture will lead to the introduction of expanded C^3 capabilities, as envisioned in the Sea Based Air C^3 Task Interim Report of OP-940.

4.4.4.2 Current Status

Efforts are on-going in the funding category 6.2 exploratory development phase. A baseline system is currently being integrated to demonstrate system feasibility. Industry has been utilized to develop breadboard hardware in a number of subsystem areas (RF front ends, signal distribution bus, narrow and wideband signal processors, etc.). A systems concept demonstration will be held in the latter part of FY-81 that will encompass narrowband waveform processing (AM, FM, single side band (SSB), LINK 4, LINK 11) in the high frequency (HF), VHF, and UHF frequency bands. In FY-82, the baseline system will be expanded to include a wideband waveform processing capability [TACAN, IFF, Joint Tactical Information Distribution System (JTIDS), GPS] and extended RF coverage into the Lx band.

4.4.4.3 Perceived Trends

One of the most appealing attributes of the TIES architecture is its adaptability to new requirements and advanced technology. The basis for this is a wideband signal distribution bus which allows a natural partitioning of RF/IF and signal processing resources. There is a natural evolution in industry toward higher levels of integration (VLSI for example) which can be readily accommodated in TIES without redesigning the system. Likewise, advances in technology which result in better performance, such as higher efficiency in a UHF power amplifier, can be integrated into TIES without a costly retrofit program. When the need arises for additional functional capability, the new modular elements (RF front ends and signal processing resources) need only to be coupled into the existing wideband distribution bus.

4.4.4.4 Areas Requiring Further Development

Current - The technology now exists to demonstrate with brassboard type hardware the feasibility and advantages of the TIES approach. Breadboards of frequency conversion units, multifunction digital signal processors, and wideband Frequency Division Multiplex (FDM) buses are currently being integrated in the TIES laboratory.

Short Term (0 to 5 years) - Development efforts over the next five years will focus on the addition of a wideband processing capability into the laboratory feasibility system to show how spread spectrum and pulse type waveforms such as JTIDS, GPS, TACAN, and IFF can be accommodated. Additional thrusts will also be made in the areas of RF hybrid technology and packaging

in general to miniaturize the system components and develop a suitable approach for airframe integration. Advanced development specifications will be written in anticipation of a five year advanced development model (ADM) program which will result in a flyable test bed system encompassing the HF through Lx frequency bands.

Mid Term (5 to 10 years) and Long Term (10 years plus) - Mid term development will be directed towards the application of maturing technologies to TIES such as fiber optics and VHSIC and the concept of a totally integrated avionics system including communications, sensors, displays and control. Ultimately, TIES hardware would be expanded to cover waveform processing beyond the basic CNI bands (10 years plus).

4.4.4.5 Development Priorities

Emphasis should be placed on transitioning the system into advanced development, and building, and testing a flyable prototype model. The benefits afforded by the architecture are platform independent, and are worth pursuing no matter who the ultimate user turns out to be.

4.4.4.6 Ongoing Program

Ties (P.E. 62721N)

Current plans call for the development of a laboratory demonstration model to be completed in the spring of 1981.

4.4.4.7 Summary

This project will provide the Navy with an advanced, modular, functionally integrated C^3NI system which is capable of meeting the projected CNI requirements of all air platforms to be introduced in the post 1990 timeframe. System feasibility will be proven within the next year using laboratory hardware and software. The advantages of this type of architecture over conventional "Black Box" integration will be clearly demonstrated. Advanced development specifications will be written taking advantage of the many lessons learned during the exploratory development phase.

5. ACQUISITION STRATEGIES

5.1 Introduction

The acquisition cycle for the development, production, and deployment of avionics equipments/systems to satisfy the needs of the Fleet is an extremely complex process, encompassing numerous managerial, business, and technical disciplines. DoD/Navy acquisition concepts, policies, and practices have continually evolved and improved. However, the pace of these improvements must accelerate during the coming years in order to keep abreast of new technologies, increased enemy threats, increased program constraints, revised business conditions, economic realities, and most importantly to shorten the development cycle such that new weapons systems can be introduced in a manner to exploit any American technology advantages. Advanced technologies, especially the electronic technologies, will continue their accelerated growth, and this growth will produce increasing obsolescence problems. The Acquisition Manager cannot control the industrial economies associated with this growth, so he must learn to plan and grow with technologies rather than oppose or ignore them. He must develop an acquisition strategy that capitalizes on technological growth, the commercial business base, and the competitive environment in order to cope with technological obsolescence, dwindling DoD budgets, inflation, and the industrial economic situation.

The acquisition strategy represents the overall plan to attain the end item objective of the acquisition process, i.e., a mature, supportable, operational system for the Fleet. It encompasses all aspects of the enterprise, including the development of technological options; test and evaluation; schedules; business base/competition considerations and strategies; data package validation methods (if applicable); contracting options; logistics support, manning, and training strategies; etc. Broadly treated at the inception of a program, where many option paths are available, an acquisition strategy evolves through an iterative process into a plan which describes the inter-weaving of business, technical, and other aspects of the program and identifies the requisite actions for achieving program objectives. The acquisition strategy is a dynamic management tool and must be kept current throughout the life of the program. The acquisition strategy must be tailored specifically for the program needs and must not be reduced to "fill-in blank" formats or "cookbooks". It is imperative that the Acquisition Manager coordinate the development of his acquisition strategy with those Project Managers who will be the equipment users, since the strategy must be consistent with the aircraft/weapon system strategy.

A key and essential decision which must be made by the Acquisition Manager as part of his initial project planning is his strategy for establishing a competitive environment for both the development and production phases of his equipment acquisition. Since the development contract is typically established through a competitive environment, the primary decision usually revolves around the question of whether to live with a sole source contractor for the life of the program or whether to establish an environment that will enable procurement of production hardware quantities from competitive sources. It is absolutely essential that the parameters impacting this decision be analyzed thoroughly early in the acquisition cycle, a decision made, and the corresponding planning developed. If the necessary planning and actions are not well thought out and accomplished early enough,

then in all probability, the ultimate and eventual decision will be one made through a matter of default. When the decision is made through default and not after conscious and thorough research and evaluation, the government usually remains completely dependent upon a sole source who, no matter how good his intention, may be unable to perform in a manner suitable to the program requirements in an economical manner. Therefore, it is imperative that the competitive strategy for both the development and production phases be established in the early planning process and so documented in the acquisition strategy.

5.2 DEVELOPMENT STRATEGY

The typical technique used to establish competition for the development phase is a negotiated procurement solicitation based on a form-fit-function performance specification. A single contract is awarded based on the evaluation of offerors technical proposals and cost proposals. A slight variation of this approach is the two-step procurement technique wherein technical proposals are submitted in the first step; and, after negotiations, cost proposals are solicited from those with acceptable technical proposals. While these approaches establish competition at the outset, they result in a sole source developer. Various techniques are available to maintain competition during the development phase. These include:

* Dual or multiple development contracts
* Teaming arrangements
* Qualified products list

It is not the intent of this document to evaluate the merits of each of these development strategies. The Acquisition Manager must evaluate the unique features and requirements of his acquisition project, and then consciously select/tailor a development strategy which suits the personality of his project. Some of the considerations that should be taken into account in formulating the strategy include the following:

* Development cost
* Technical risk
* Anticipated technology and item complexity
* Development schedule
* Project criticality (mission essential)
* Mobilization requirements
* Long term support needs and logistics/maintenance factors
* Capital investment requirements
* Qualification requirements/costs
* Industry market conditions

An alternate strategy is development of the equipment/system by an in-house field activity/laboratory culminating in the availability of a validated design-disclosed data package which can be used for industry procurement of production quantities on a low risk, configuration-controlled competitive basis. In-house development may in certain instances be the preferred approach based on schedule constraints, standardization requirements, or specialized/unique in-house knowledge.

5.3 PRODUCTION STRATEGY

Initial production quantities will normally be provided by the development contractor. Several techniques are available to achieve competition during follow-on production. These include:

* Competition among multiple developers or teams (where these approaches were used during the development phase)
* Reprocurement using a validated design-disclosed data package
* Competition among qualified products list sources
* Leader-follower concept
* Reprocurement using a form-fit-function performance specification

Again, the Acquisition Manager must evaluate the unique features and requirements of his acquisition project, and then consciously select/ tailor a production strategy which suits the personality of his project. If he determines that reprocurement using a validated design-disclosed data package is the preferred strategy, then he must assure that adequate data and their associated data rights have been specified in the development contract and that these data are validated prior to follow-on procurement. Some of the considerations that should be taken into account in formulating the strategy include the following:

* Design ownership and its associated costs
* Data package availability and completeness
* Data package suitability for competitive acquisition
* Proprietary data rights and patent restrictions
* Design stability and technical risk
* Design technology and item complexity
* Standardization
* Quantities to be procured over the life cycle
* Estimated unit costs (with and without competition)

* Schedule or delivery requirements and needs for multi-year procurements

* Urgency of needs

* Project criticality (mission essential)

* Production capacities versus required production rates and industrial base availability

* Mobilization requirements

* Long term support needs and logistics/maintenance factors

* Capital investment requirements

* Qualification requirements/costs
* Potential risks for and significance of program failure

* Industry market conditions

5.4 SUMMARY

It is essential that each project be supported by a documented acquisition strategy. These strategies must identify the techniques to be used for establishing a competitive environment for both the development and production phases. The need to develop these strategies as part of the initial project planning is paramount. These strategies must take into account the considerations listed under the development and production strategies. Each of these considerations may be volatile depending upon the sponsoring activity, project constraints, political environment, and the time within the acquisition cycle when the acquisition method decision is made. In general, the earlier within a project that each issue is identified, analyzed, and addressed, the better the prospects for a successful project. This is true not only from the standpoint of being able to preplan, but from the standpoint of political risk as well. An early decision point and acquisition scenario definition allows time to budget properly and to bring the parties involved in the acquisition process to an understanding of the acquisition plans; both elements serve to mollify opposing views and assure continued agreement with the proposed project direction.

6. CORE AVIONICS PLANS

Core avionics systems perform functions that are required in most, if not all military aircraft. All aircraft must take off and land, be stable in-flight, communicate with ground stations and other aircraft, and navigate from point to point.

Core avionics can be defined as those avionics systems/equipments which are used primarily for operation of the aircraft, including take-off, flight, navigation, return-to-base, and landing. Core avionics equipment typically includes computers; instrumentation, controls and displays; navigation systems; and communications systems. In a military aircraft, core avionics are complemented by mission avionics, which are those avionic systems/equipments that are used primarily to accomplish a specific military mission, e.g., anti-submarine warfare (ASW), airborne early warning (AEW), etc.

The responsibility for the conceptual development and acquisition of Navy avionics systems in the Naval Air Systems Command has been assigned between two separate organizations, one for core avionics (AIR-533) and one for mission avionics (AIR-549). Future editions of the NAVAIR Avionics Master Plan will address both core and mission avionics long range planning issues in support of the mission of these organizations. This first edition addresses only salient topics of core avionics planning.

6.1 TACTICAL COMMUNICATIONS

Voice communication remains a mainstay of tactical operations. Aircrews rely heavily on their UHF-AM radio circuits for all phases of air operations; the radio is flight essential equipment. A number of improvements to existing voice circuits are emerging from developmental stages and are taking their place in the Fleet inventory.

Recent joint operations have demonstrated the need for interoperability between ground forces, using primarily VHF-FM circuits, and air elements, using primarily UHF-AM circuits. The need for civil air traffic control communications capability in military aircraft is evident. The AN/ARC-182(V) combination UHF/VHF - AM/FM Radio Set focuses on these needs.

Tactical communications circuits are subject to intercept and exploitation. New families of voice cryptographic equipments that will minimize such exploitation are now available from NSA to interface with tactical radio sets. Electronic countermeasures sets designed to jam voice communications are common in the inventories of many of our potential enemies. Spread spectrum techniques and other anti-jam (AJ) precautions are being implemented in a number of the new tactical communications sets. A modem is being developed for the AN/ARC-182(V) Radio Set family that will be suitable to interoperate with planned Army and Air Force AJ communications systems.

The advent of computer technology has fostered the growth of digital data communications technology. Systems such as Link 4A and the Joint Tactical Information Distribution System (JTIDS) provide digital data communications between military platforms for a number of Communications, Command and Control (C^3) applications.

The modern architectures of internal communications systems call for multiplexed serial data bus designs, as opposed to the older hardwired point-to-point wiring methods. The currently available data bus standard, MIL-STD-1553B, limits data rates to one megabit/sec. This is suitable for many functions found within a modern jet aircraft for control loops. Potentially wider bandwidth sensor and control systems will require an expansion of this data rate requirement.

Earth orbiting satellite radio repeater systems now provide world wide, real time communications circuits to even the smallest military units. The need therefore exists for the development of small, light weight, environmentally rugged military satellite terminal equipments. Many other forms of line of sight (LOS) and land-line communications circuits can be interfaced with satellite relay terminals to provide effective command and control.

The following articles present a number of significant issues relating to Navy tactical communications equipments and systems that must be planned for and implemented in Fleet hardware. These articles describe some of the significant design programs and hardware implementation efforts that will provide an enhanced tactical communications capability to the Fleet for the next decade and beyond. Systems Command avionics managers should key acquisition budgets and time schedules to these developments. As new Fleet needs are identified, new task elements will be defined and incorporated in subsequent issues of this NAVAIR Avionics Master Plan.

6.1.1 COMMUNICATION, COMMAND, AND CONTROL (C^3) ANALYSIS

6.1.1.1 Background

Analysis techniques have long been used to determine the operational requirements for military weapon systems. The basis for the system requirements originate with the threat which the weapon system was anticipated to encounter during the lifetime of the system. Weapon systems are evaluated by such measures of effectiveness as probability of kill, hits on force, and probability of survival. Frequently in the past, communications systems were assumed to operate flawlessly in these analysis scenarios, and the effects of intentional jamming, deception, and interoperability were frequently neglected. The specifications for communication systems were generally driven by the current state-of-the-art, theoretical noise limitations, propagation characteristics, and (in the instance of some digital communication links) on the amount of information required to perform a mission expressed as a data rate. It should be noted that weapon system performance degradation due to communication system breakdown was never analyzed.

6.1.1.2 Current Capability and Identified Deficiencies

The current C^3 analysis effort is attempting to determine the impact communication system effectiveness and communication system architecture have upon carrier group operations. Monte-Carlo simulation models are being devised to simulate attacks upon the carrier group by hostile forces. The scenarios being studied are similar to those depicted in a report entitled "(S) Naval Airborne and Surface Threats for Evaluation of F-14 Airborne Weapon

System 1985-2000 (U)" NADC 77248-50 of 30 September 1977. The threat information was compiled from Air Force and Naval intelligence reports such as the Naval Intelligence Command report "(S) Soviet Airborne Noise Jamming Threat as related to U.S. Navy Systems (U)", NIC-1732R-004-78 of December 1978.

6.1.1.3 Equipment Development and Modernization

Studies affecting present communication systems, and systems which are planned to be introduced into the Fleet include:

* UHF/VHF communications [AN/ARC-159(V), AN/ARC-182(V)]

* Advanced UHF systems (SEEK TALK, SINCGARS, spread spectrum modems, etc.)

* Joint Tactical Information Distribution System (JTIDS) net management

The UHF/VHF systems deployed in the Fleet will be analyzed for performance against current and projected threats. Suggestions for changes to operational usage may be made as a spin-off of these studies, if they are deemed necessary. The advanced UHF systems will be analyzed and evaluated in a similar manner, and recommendations made where appropriate. The largest continuing effort of C^3 analysis is in the area of JTIDS net management. These studies will define the information handling procedures, relay capability requirements, and net control philosophy for the JTIDS system in various military operation theaters.

6.1.1.4 Summary of Requirements

Short Term (0 to 5 years) - Short term requirements are as follows:

* Consolidate accurate threat jamming capabilities.

* Determine valid scenarios for communication system analysis.

* Improve the command and control requirements data base (C^2RDB).

* Perform preliminary JTIDS and UHF/VHF analysis.

* Perform preliminary advanced UHF systems analysis.

Mid Term (5 to 10 years) - Mid term requirements are as follows:

* Maintain the C^2RDB.

* Maintain consolidated threat jamming information documents.

* Perform JTIDS net management studies.

* Evaluate advanced systems requirements/performance.

Long Term (10 years plus) - Long range plans call for maintaining the C^3 data base and consolidating/updating threat jamming capability information.

6.1.1.5 Development Priorities

The analysis of JTIDS capabilities and implementation alternatives in regards to net management should receive the highest priority in the near term. Other items which then should receive attention are the C^2RDB and advanced UHF systems analysis.

6.1.2 RADIO SET AN/ARC-182(V)

6.1.2.1 Background

Current operational scenarios dictate the following avionic communications requirements to operate the air vehicle and/or to support the accomplishment of a specific military mission; e.g., ASW, AEW, etc.

* Direct VHF (FM) communications capability between tactical aircraft providing close air support and ground combat forces.

* VHF (AM) and UHF (AM) communication capabilities for safety of flight and compatibility with commercial/international airways.

* UHF (FM) for secure voice.

* VHF (FM) maritime mobile band is required for safety and certain tactical situations.

6.1.2.2 Current Capabilities and Identified Deficiencies

Two or more of the existing tactical radio sets are required to meet most of these needs, but fail to provide all the capabilities needed. These existing radio sets are:

* AN/ARC-114A, AN/ARC-115A, AN/ARC-159(V), and AN/ARC-186(V).

Current operational deficiencies encountered with these existing radio sets and respective antennas are:

* They are too heavy and require too much space.

* They do not have anti-jam (AJ) capabilities.

* They have deficient reliability characteristics.

* Multiple antennas are required to cover the wide frequency range.

6.1.2.3 Equipment Development and Modernization

The Radio Set AN/ARC-182(V) is the Navy's most recent tactical radio for AM/FM/VHF/UHF communications capability. This Radio Set is a solid state airborne tactical communications transceiver capable of both non-secure and

secure voice and digital data transmission and reception. It is being developed to be form and fit compatible with the Radio Set AN/ARC-159(V) and will provide interoperability with Army/Marine ground units, civil air, maritime, NATO, and conventional UHF participants. This single Radio Set functions in both AM and FM modes of operation in the following bands:

* 30 - 88 MHz FM VHF for ground force tactical communications,
* 108 to 156 MHz AM VHF for air traffic control,
* 156 to 174 MHz FM VHF for maritime mobile, and
* 225 to 400 MHz AM/FM UHF for tactical air-to-air and air-to-surface.

The basic radio set operates on over 11,000 channels with 25 KHz channel spacing. Wideband digital data modes are also possible with the set. Encryption of voice signals is possible with the use of a companion communications security (COMSEC) device. The radio is suitable for operation with the KY-28/URA-5 Coder and the KY-58/GRT Keyer. This radio is intended as a functional replacement of the AN/ARC-114A, AN/ARC-115A, AN/ARC-159(V)1, AN/ARC-159(V)2, and AN/ARC-186(V) radio sets. A single airborne antenna, usable over the 30-400 MHz frequency range, will replace multiple existing antennas.

The AN/ARC-182(V) is now in full scale development. Ten developmental units have been delivered to the Navy for Technical Evaluation (TECHEVAL), with Operational Evaluation (OPEVAL) scheduled for January 1981 through June 1981. Approval for Service Use (ASU) is anticipated in late 1981 with production deliveries of approximately 1,000 radios per year scheduled over the period of 1982 to November 1986. Initial Operational Capability (IOC) is scheduled for 1982.

The initial application for this versatile Radio Set is the F-18 aircraft. Current planning indicates that the AN/ARC-182(V) family of radio sets will be suitable for new applications and retrofit into over thirty different types of Navy aircraft plus selected NATO and other foreign military applications. The use of a "common radio" will substantially enhance interoperability among international forces.

Currently, the radio is being adapted to accommodate an anti-jam (AJ) spread spectrum mode of operation. This capability will be housed in a separate add-on modem unit. In addition to SINCGARS V compatibility in the VHF band, the modem will provide an AJ and data capability in the UHF band. The modem has a planned IOC of 1985. This modem will also provide interoperability with Air Force HAVE-QUICK ECCM system.

6.1.2.4 Summary of Requirements

Short Term (0 to 5 years) - New production AN/ARC-182(V) radio sets providing VHF/UHF/FM/AM communication capabilities for both secure and non-secure voice and digital data are needed for both new aircraft and for retrofitting existing aircraft to replace obsolete radio sets.

Mid Term (5 to 10 years) - Navy radio sets must have ECCM capability interoperable with Army SINCGARS V, and Air Force HAVE-QUICK systems.

Long Term (10 years plus) - It is probable that changes will be required to improve performance, reliability, and maintainability. Changing ECCM environments and tactical scenarios will require modifications to the current AN/ARC-182(V) performance baseline. The architecture and package design of the radio set should be such that these modifications can be retrofitted without redesign of the radio set.

6.1.2.5 Development Priorities

* Development of the AJ modem to provide ECCM capability.

* AN/ARC-182(V) improvements to enhance performance, improve reliability, and provide second sources for critical components.

  * Development of second source for hybrid power amplifiers and increase output power to 100 watts.

  * Development of second source for SOS LSI chips in the frequency synthesizer.

  * Improvement of intermediate frequency (IF) filtering to allow adjacent channel operation.

* Long range improvements to maintain technology currency, achieve increased volumetric efficiencies, achieve increased reliability and enhance frequency hopping capability. Because of the AN/ARC-182(V)'s modular construction, these should be achieved in stages without complete redesign and replacement of the radio.

* Development of compatible adaptive null antenna arrays for additional ECCM protection.

6.1.3 INTEROPERABILITY OF SINCGARS, HAVE-QUICK, AND AN/ARC-182(V)

This article is classified.
Refer to the classified supplement.

6.1.4 ANTI-JAM (AJ)/SECURE/CONFERENCING MODEM

This article is classified.
Refer to the classified supplement.

6.1.5 ANTI-JAM (AJ) COMMUNICATIONS

This article is classified.
Refer to the classified supplement.

6.1.6 JOINT TACTICAL INFORMATION DISTRIBUTION SYSTEM (JTIDS)

6.1.6.1 Background

JTIDS, a tri-service program which is being developed to significantly upgrade tactical communications, is an integrated communications, navigation and identification system based on Time Division Multiple Access (TDMA) technology. To meet its requirements for greater data capacity, the Navy is developing an enhanced technology known as Distributed TDMA (DTDMA). The JTIDS system will support Naval air, surface and submarine combat operations and will be interoperable with other services and NATO countries utilizing JTIDS.

6.1.6.2 Current Capability and Identified Deficiencies

Combat experience gained during the Southeast Asia conflict and Mideast incidents exposed several deficiencies in the Navy's tactical communications, navigation and identification systems. Extensive analysis of the combat situations indicated that a reliable, rapid access, high capacity, secure and jam resistant communication link was necessary to enhance mission execution and reduce losses due to hostile actions. JTIDS is being developed to provide that communication link.

6.1.6.3 Equipment Development and Modernization

JTIDS is a line of sight (LOS) system which provides secure, high speed, anti-jam, low probability of intercept/exploitation means of communications suitable for use in both digital and voice applications. Extended LOS (ELOS) capabilities are to be provided through the use of airborne relays. Initial implementation of JTIDS will provide AJ Communications of Link 4, Link 11 data, and voice in addition to relative grid navigational positions of platforms and automatic identification of friends. The JTIDS terminal will also perform the normal TACAN function. The amount of digital data which can be passed by JTIDS is a function of the terminal size, platform configuration, and particular technology, but even in minimum applications, it will exceed the capabilities of current systems that serve existing combat direction systems. JTIDS voice capabilities will include demand access, conferencing, and priority interrupt features in order to provide users with immediate access when required for threat warning and weapons direction.

OPNAV Instruction C3510.13 contains the policies and guidance on the Navy implementation of JTIDS.

6.1.6.4 Summary of Requirements

Short Term (0 to 5 years) - The short term requirements for the Navy JTIDS Program are to complete the Advanced Development phase and initiate the Full Scale Development (FSD) phase of the program.

MILESTONES

Complete Advanced Development testing	Jun 81
Complete FSD Terminal design studies	Dec 81
DSARC II decision	Oct 81
Award FSD Terminal contract	Dec 81
1st Terminal delivery	Mar 84
Complete Navy Preliminary Evaluation (NPE)	Nov 85

Mid Term (5 to 10 years) - The mid term requirement for the Navy JTIDS Program is to obtain approval for service use (ASU) for JTIDs on the F-14, F-18, E-2C, and CV types of platforms. The initial operational capability (IOC) for a carrier task force has been established as the last quarter of CY 87.

MILESTONES

Complete Navy Technical Evaluation (NTE)	Jun 86
Complete Operational Evaluation (OPEVAL)	Mar 87
Obtain ASU	Jul 87
DSARC III decision	Oct 87
IOC	Nov 87

Long Term (10 years plus) - The long term requirement for the Navy JTIDS Program is the complete integration of JTIDS terminals into all platforms designated by OPNAV Instruction C3510.13.

6.1.6.5 Development Priorities

Full scale development of the DTDMA terminal is of prime importance. In parallel with the terminal development, integration concepts which make maximum utilization of the JTIDS functions and further definition of the relative navigation mechanization must be given equal importance.

6.1.7 ADAPTIVE ANTENNA ARRAYS

6.1.7.1 Background

Most UHF and VHF airborne communications antennas in current use consist of a simple broadband monopole element with the metal skin of the airframe used as a ground plane. Other types of simple antennas are also used in special applications, such as helicopters. Continuously-loaded whip antennas allow for "mechanically short", but electrically resonant, antenna designs. The goal of most antenna designs is to achieve omnidirectional coverage such that the aircraft structure does not contribute to radio signal variation.

Even though the non-uniform ground plane provided by an aircraft distorts a true omnidirectional antenna pattern, many antenna designs can provide nearly omnidirectional coverage. An inherent disadvantage of omnidirectional coverage is that the antenna also looks toward potential jamming sources at the same time that it is looking toward the intended signals. In a tactical environment, intentional jamming is a vital concern.

6.1.7.2 Current Capability and Identified Deficiencies

Technology exists to design practical adaptive null antenna arrays that can be placed on Fleet aircraft. These adaptive arrays can sense the direction of the desired signals and selectively null out undesired signals. The desired signals have to be uniquely encoded for identification. An array of several individual antenna elements provides phase and amplitude information to an antenna signal processor. Through the use of appropriate signal processing algorithms, unwanted signals are phase-nulled from the receiver input.

Various avionics designers have produced developmental systems to demonstrate the feasibility of adaptive-null antenna arrays. Problems still remain in refining these designs to be suitable for quantity production and, at the same time, be aerodynamically suited for high performance aircraft.

Adaptive antenna arrays have application to a number of tactical communications systems. Some of these systems are:

* Radio Set AN/ARC-182(V)
* Advanced Sonobuoy Communications Link (ASCL)
* Joint Tactical Information Distribution System (JTIDS)
* Anti-Jam Link 4 applications
* New Identification, Friend or Foe (IFF) Systems, such as United States Identification System (USIS)
* HF communications
* Future anti-jam spread spectrum voice and data communications systems

6.1.7.3 Equipment Development and Modernization

At the present time there are no airborne phased array antenna systems in Fleet use, however, there are several systems currently under 6.2 development and/or study. The system which is closest to Fleet deployment is the adaptive phased array antenna for the ASCL sonobuoy receiver. This system is currently in a pre-production phase, and is slated for introduction to the Fleet with the P-3C Update III weapon system. A flight test program for FY 81 will test an adaptive antenna system for the AN/ARC-182(V) multi-band radio that is based upon an adaption of the Air Force antenna system developed for the SEEK TALK/HAVE QUICK Program. In addition, a development contract has been awarded for a military Lx-band phased array to enhance the AJ performance of a tactical JTIDS terminal. A high frequency (HF 3-30 MHz) adaptive antenna system was flight tested in FY 80. This program successfully demonstrated an adaptive HF antenna receiver function, but the program was discontinued due to funding constraints.

6.1.7.4 Summary of Requirements

Short Term (0 to 5 years) - Initial applications of adaptive null antenna systems will be enhancements to existing communications systems such as the Radio Set AN/ARC-182(V) or the older AN/ARC-159 UHF-only radio set. As such, the following requirements for these and other proposed systems must be identified:

* Spatial and spectral coverages

* Number of expected jammers

* Magnitude of the jamming environment

Mid Term (5 to 10 years) - As adaptive null antenna systems mature, these systems may potentially be applied to all tactical aricraft. Additional factors must be considered including physical size and weight constraints. A HF adaptive antenna system for the AN/ARC-182 will be ready for advanced development. Likewise, the JTIDS adaptive array will be under development.

Long Term (10 years plus) - In the long term, it is difficult to forecast the future of adaptive antenna techniques. Other technologies, such as laser transmission systems and direct satellite relay, may make conventional VHF and UHF radio systems less vital as a means of tactical communication. However, to allow the adaptive array technology to be of maximum benefit, an integrated antenna processing approach is required for UHF through L band communications bands. This is dictated because of their cost and size.

6.1.7.5 Development Priorities

Short term development priorities should address broadband frequency independent antenna systems. Currently, a single transceiver can operate over a 30 to 400 MHz band with 25 KHz channel spacing. In the order of 11,000 channels can be generated and received in an equipment that can be hand-held. Antenna systems that have consistent gain and impedance characteristics over this band are not currently available to function with this radio set. When single element high performance antenna components are developed, they can then be applied to adaptive array designs. A 6.2 program should be started to design an adaptive array to cover the UHF/VHF communications, JTIDS, TACAN and GPS functions.

The field of active antenna element designs should be reviewed for possible application to adaptive arrays.

Development funds should be focused on specific applications of existing technology. Small airframes associated with carrier-based air operations present the largest challenge to the application of adaptive antenna arrays. Attack aircraft, such as those used by the Marine forces, probably have the most urgent need for jam-resistant communications systems.

6.1.7.6 Ongoing Programs

JTIDS Adaptive Array (P.E. 62721N)

The object of this program is to construct and flight test a feasibility model in FY 82.

AN/ARC-182 Adaptive Array (P.E. 62721N)

The aim is to test and evaluate the performance of a modified HAVE QUICK antenna on the AN/ARC-182 radio.

HF Adaptive Array (P.E. 62721N)

The HF adaptive array program is to provide an airborne HF adaptive array. The project is currently not funded but should be continued.

6.1.8 HIGH POWER TUNABLE FILTER

6.1.8.1 Background

On those aircraft that share a number of Radio Frequency (RF) emitters, the electromagnetic environment is extremely severe and complex. Intermodulation products of the intended emissions contribute to this complexity. Almost all RF transmitters produce a low-level, side-band noise spectrum at the same time they produce the on-channel signals. The spurious signals generated in modern transceivers are particularly high resulting in poor out-of-band spectral control. When the platform also has sensitive receivers on board, certain precautions must be taken to limit the intermodulation and side band noise inputs to these receivers.

6.1.8.2 Current Capability and Identified Deficiencies

On current Fleet aircraft, such as the E-2C, cavity type UHF bandpass filters are used on the output of the various transceivers to limit sideband noise output of the transmitters. In addition they exclude other off-channel emissions from the receiver unit. These filters currently are mechanically tuned by servo systems and about 10 seconds are required to change frequencies.

As frequency-hopping methods are introduced into systems to provide jam-resistance improvements, the cavity-type filters currently used will be replaced by faster tuning units. Electronically tuned varactor filters are currently available. However, the nonlinear voltage versus capacitance curve of this device limits the power handling ability of this type of filter.

Another approach to tunable filters is the use of pin diode switched capacitor arrays. This approach promises greater power handling capability, fast tuning times and compatibility with digital control. Tunable filters using this approach have been fabricated. These filters operate in the UHF frequency band and demonstrate the feasibility of the approach. Additional efforts are underway to broaden the frequency coverage to include the VHF as well as the UHF frequency band.

6.1.8.3 Equipment Development and Modernization

High power electronically tuned filters are under investigation by several communications avionics vendors. Developmental units have been demonstrated. It is anticipated that production quantities of electronically tuned filters (UHF) will be available in the next three to five years.

Special filters that cover both the VHF and UHF tactical communications bands must be developed for use with the radio set AN/ARC-182(V). These developments must be supported now in order to realize operational systems in the next 5 to 10 years. The rapid tuning rates required by frequency hopping systems must be explored. New technology areas including microwave integrated circuits and surface acoustic wave devices should be investigated to find better solutions to these problems.

Long term solutions to on-board radio frequency interference may come about from vastly different approaches to frequency generation and emission management. On-board computers would select optimum communications channel combinations. Predicted interference patterns would be suppressed dynamically.

6.1.8.4 Summary of Requirements

Short Term (0 to 5 years) -

* Improve pin diode and capacitor components to achieve a wider tuning range, narrower bandwidths, and higher power handling capabilities.

* Continue development of high power electronically tuned filters for both the VHF and UHF bands.

* Commence development of advanced frequency management concepts using computer prediction of interference patterns and selections of optimum communication channel selection.

Mid Term (5 to 10 years) -

* Develop miniature components and packaging concepts.

* Incorporate advanced electronically tuned filters into Fleet equipments.

* Continue development of advanced computer controlled frequency management techniques.

Long Term (10 years plus) -

* Introduce advanced computer controlled frequency management techniques into Fleet equipments.

6.1.8.5 Development Priorities

Developments should focus on expansion of existing loaded cavity filter designs using semiconductor switching devices for tuning with lumped constant components. New areas of technology should be explored for high power applications. Long term planning should include analysis of dynamic suppression frequency management methods and hardware implementations.

6.1.8.6 Ongoing Program

Filter Development (P.E. 62721N)

The purpose of this task is to develop a high power electronically tunable filter. Effort is in progress to develop a laboratory VHF/UHF filter for delivery in late FY 81.

6.1.9 IDENTIFICATION FRIEND OR FOE (IFF)

This article is classified.
Refer to the classified supplement.

6.1.10 UNITED STATES IDENTIFICATION SYSTEM (USIS)

This article is classified.
Refer to the classified supplement.

6.1.11 MULTIMODE RECEIVER (MMR)

6.1.11.1 Background

The Multimode Receiver (MMR) is a precision landing system receiver that decodes and processes guidance signals for instrument approach and landing of both fixed and rotary wing aircraft. The system will provide the airborne subsystem functions of the following landing systems:

* Instrument Landing System (ILS)

* Microwave Landing System (MLS)

* Pulse Coded Scanning Beam (PCSB)

  - Marine Remote Area Approach and Landing System (MRAALS)
  - C-Scans

The MMR is designed to operate in either a stand-alone or integrated aircraft installation. In the stand-alone installation, outputs will be directly wired to analog and digital displays. In the integrated aircraft installation, equipment outputs will access displays via a MIL-STD-1553 serial digital multiplex data bus. The MMR does not include a precision distance measuring equipment (DME) system; however, it will be capable either of processing onboard TACAN signals to obtain precision range data or by directly utilizing range and range-rate data from a separate onboard DME system.

6.1.11.2 Current Capability and Identified Deficiencies

The MMR program is currently entering full-scale development. A production decision should be made in early FY 83. In addition no OPEVAL dates have yet been established nor are there plans to consider a mass-retrofit to existing platforms.

6.1.11.3 Equipment Development and Modernization

The MMR system is currently in full-scale development. Decisions regarding equipment development and modernization should be in consonance with the production decision slated for early FY 83.

6.1.11.4 Summary of Requirements

The MMR is presently a requirement for CH-46 and CH-53 helicopters. The MMR is considered as additional equipment and will not replace existing equipment on these aircraft.

6.1.11.5 Development Priorities

During the full-scale development phase of the MMR program, the following technology items should be addressed:

* Microwave receiver RF technology,
* Large Scale Integration (LSI),
* Electromagnetic compatibility,
* Thermal design and packaging, and
* Hybrid circuit design.

6.1.12 SATELLITE COMMUNICATIONS TERMINAL

This article is not available, and will be provided at a later date.

6.1.13 INTERCOMMUNICATIONS SYSTEM (ICS)

6.1.13.1 Background

The aircraft Intercommunication System (ICS) provides audio communications among crew members, radios, and mission related equipment. Traditionally, each new aircraft has been accompanied by the development of a new ICS or an extensive modification of an existing system. The existing systems are all-analog and were developed with little commonality. Six types of ICS systems are currently used on Navy/Marine aircraft. Under the Avionics Components and Subsystems (AVCS) Program, the Navy is developing a standard, digital voice ICS that is compatible with MIL-STD-1553, is TEMPEST-qualified, and provides for reduced size, weight and power consumption.

6.1.13.2 Current Capability and Identified Deficiencies

Current deficiencies of Fleet ICS equipment are as follows:

* Non-compliance with TEMPEST requirements,

* Excessive size, weight and power consumption,

* Obsolete technology,

* Proliferation of equipment, thus requiring many types of spares,

* High skill level of maintenance personnel required, and

* High cost for logistics support.

Existing ICS are analog systems that are predominantly connected by parallel wiring, although some use a central switching matrix configuration. The parallel shielded wiring in Fleet systems represents a significant size and weight burden to the weapon system platform. In spite of additional Electro-Magnetic Interference (EMI) precautions to prevent cross-coupling of signals, significant TEMPEST problems are generated by the long runs of parallel wiring. Additionally, installation practices for current ICS systems cause potential TEMPEST violations, and thus each aircraft must be individually certified for TEMPEST compliance. This is due to the fact that existing ICS installations, by virtue of system design and random variations from airframe to airframe, are not inherently TEMPEST compliant and even a minor connector or wire repair often necessitates a TEMPEST recertification of the entire aircraft.

Central switching matrix configurations, while less sensitive to installation problems, are subject to failures of the central units. These systems are not distributive in nature and are not fault-tolerant or auto-reconfigurable. If considerable expansion of the communications subsystem is required, these ICS must be extensively modified or redesigned to provide the required capabilities. Presently, little or no commonality of ICS equipments exists between aircraft types, thus necessitating large inventories of ICS spares in the Fleet.

6.1.13.3 Equipment Development and Modernization

The digital voice ICS is composed of one or more master control stations, remote crew stations, and one secure and one non-secure radio interface units. Although the mix and number of these ICS units will vary for aircraft type, each of these units can be common to multiple aircraft, requiring only minor differences that can be programmed into the units. The inclusion of Integrated Radio Controls (IRC) into this system, which can be easily accomplished utilizing the MIL-STD-1553B data bus, can provide even greater reductions of size and power consumption. This ICS will also have provisions for digitally generated voice to annunciate warnings and alarms, thus providing compatibility with the next generation of avionics instrumentation.

The digital voice ICS required to meet the operational communications needs of the Fleet will require the following features:

* MIL-STD-1553B data bus compatible architecture,

* Option for fiber optic data bus and interconnections,

* Inherent TEMPEST compliance with minimal TEMPEST sensitivity to different installations,

* Remote control of aircraft radios,

* Distributed processing for system control and auto-reconfiguration,

* Solid state technology, and

* Commonality and supportability by maximum utilization of common Shop Replaceable Assemblies (SRAs).

The inclusion of IRC in the ICS represents a significant step in integrating previously related but separate functions into one system, thus reducing the combined weight, volume, and power used in the weapons system. Use of a distributed processing architecture can greatly enhance the survivability of the system without size, weight, or power penalties. This feature can allow the system to degrade gracefully in the presence of faults or damage by reconfiguring the system data transfer functions. The use of up-to-date technology will allow size and weight reductions of more than 30% and power consumption reductions of more than 60%, as compared to existing installations. The utilization of the MIL-STD-1553B data bus for interconnections will result in greatly reduced cabling complexity. Incorporation of multinodal fiber optic interconnections with the MIL-STD-1553B format and the distributed processing control capabilities of this digital voice ICS can result in a highly survivable system that is more affordable from the standpoint of installation, maintenance, and logistic support than current systems.

A prototype multiplexed digital voice ICS has been developed under the AVCS program to assess important system design parameters and trade-offs; e.g., voice digitization techniques, sampling rates, and voice bandwidths. This equipment utilizes the MIL-STD-1553B data bus, and has undergone intelligibility testing in aircraft acoustic noise environments at the Air Force Medical Research Laboratory as part of the Tri-Service coordination effort. Close coordination has been maintained with the Air Force and the Army during the development and testing of the digital voice ICS. Potential applications of the digital voice ICS include the following aircraft:

A-6E	H-1/H-3	VCX
EA-6B	S-3A	ECX
C-2	OV-10A	MPA
E-2C	SH-60B	

6.1.13.4 Summary of Requirements

Short Term (0 to 5 years) - Short term plans include:

* Continued Tri-Service coordination on ICS

* Completion of the following investigations:

  - Low bit-rate voice digitization
  - Radio interface characterization
  - Secure Communications (RED and BLACK) techniques
  - Voice recognition and generation compatibility with digital voice systems.

* Complete the ICS performance specification

* Complete the development of the multiplexed digital voice ICS

* Complete ICS TECHEVAL, OPEVAL, and ASU requirements

Mid Term (5 to 10 years) - Based on completion of the short term tasks, it is planned to:

* Evaluate use of a complete digital voice ICS on each model of Navy/Marine aircraft.

* Incorporate the multiplexed digital voice ICS into new aircraft and applicable aircraft undergoing CILOP.

Long Term (10 years plus) - The long term efforts will:

* Investigate expansions of ICS distributed control architectures into non-audio portions of the communications subsystem.

* Develop ICS distributed control architectures with maximum commonality of hardware with the multiplexed digital voice ICS.

6.1.13.5 Development Priorities

The highest priority tasks are to:

* Complete development of the multiplexed digital voice ICS.

* Complete TECHEVAL, OPEVAL, and ASU of the ICS.

* Incorporate digital ICS into Fleet aircraft.

6.1.13.6 Ongoing Programs

Standard digital voice Intercommunications Systems (ICS) development (P.E. 64203N)

The purpose of this task is to develop a standard digital voice ICS that will replace existing analog voice ICS, which have serious operational deficiencies and are difficult to support. This new standard system will reduce size, weight, and power consumption of ICS while providing substantial performance improvements.

MILESTONES

FY 81	
Hardware Investigations	Sep 81
Draft Specification	Sep 81
FY 82	
Initiate Voice Recognition and Synthesis (VRAS)	Oct 81
Integration Investigations	Oct 81
Demonstration Hardware	Sep 82
FY 83	
Continue VRAS Investigations	Oct 82
Final Development Specification	Mar 83
Request for Authority to Negotiate (RAN) Submission	Mar 83
RAN Approval	Sep 83
FY 84	
Initiate Investigations into [illegible] Communications Areas	Oct 83
Request for Proposal (RFP) Release	Oct 83
ICS Hardware Development Contract	Sep 84
FY 85	
First Article Delivery	Aug 85
FY 86	
TECHEVAL Complete	Dec 85
OPEVAL Complete	Aug 86
Production Readiness Review (PRR)	Sep 86
FY 87	
Approval for Service Use (ASU)	Dec 86

6.2 NAVIGATION

With the continuing growth in system design complexity, the navigation requirements of present and future aircraft must be carefully analyzed in view of the constraints imposed by time, technology and cost. It has become obvious that no single system can satisfy all requirements simultaneously. Consequently, one must select a combination of systems that can best meet specific aircraft requirements for the least cost.

There is a great variance in the navigation requirements of the various types of military aircraft. This wide range of requirements has resulted in the development of a variety of navigation sensors with an equally wide range of performance characteristics. When they are properly integrated into a system, their different characteristics tend to complement one another. The availability of this wide range of sensors allows the navigation system designer to chose a system configuration which best meets his requirements.

The advent of the small lightweight airborne digital computer has made it possible to develop a totally integrated navigation system that will take advantage of the complementary nature of the performance characteristics

of different navigation sensors. This is accomplished through use of a computer software algorithm known as the Kalman filter, which uses the complementary information contained in the outputs of the different sensors to estimate and then correct the systematic errors which are present in the individual sensor outputs. Optimum navigation can be achieved by integrating a self-contained navigator, such as an inertial navigation system, with an external geodetic navigation reference and a relative (tactical) navigation reference.

Future inertial navigation systems will more completely exploit strapdown mechanizations in conjunction with solid state gyros. The strapdown system technology will also pave the way for the development and utilization of a strapdown navigation sensor package totally integrated with the aircraft avionics. This new system approach promises to eliminate the duplicate sensor assemblies of different aircraft functions and provide a highly dependable, cost effective, redundant source of inertial data for aircraft navigation, weapon delivery, and flight control.

The following sections will detail the anticipated developments in self-contained, geodetic, and relative navigation systems into the 1990's.

6.2.1 INERTIAL NAVIGATION

6.2.1.1 Background

Navigation has become an integral and important aspect of the command and control (C^2), strike coordination, weapon delivery and surveillance functions performed by current Navy fixed and rotary wing aircraft. The navigation function can be best performed by a complementary array of equipment consisting of the Global Positioning System (GPS), OMEGA, TACAN, and doppler radars, and Inertial Navigation Systems (INSs).

Currently, the INS is the only available self-contained, non-radiating, non-jammable navigation device that can provide the required aircraft reference data for both navigation and weapon delivery (i.e., simultaneous and instantaneous aircraft velocity, attitude, heading and position). The advantage of the INS, however, is hampered by the lack of instant turn-on capability when compared with other navigation systems, such as OMEGA, TACAN, etc. The INS must be aligned before it can provide accurate aircraft reference data; the accuracy of which is a function of the alignment quality. Essentially, the alignment of an inertial system consists of determining the level coordinate frame and true North by sensing gravity and earth's rate. Once alignment is complete the INS senses vehicle acceleration and provides the required outputs. For Navy application, the alignment of the INS is complicated by being performed on a moving base (an aircraft carrier), and this requires reference data from the Ship's Inertial Navigation System (SINS).

This alignment process is performed in the INS's computer, with an optimal Kalman filter which uses input data from the SINS. Alignment data are transmitted from SINS to the INS via the Navy Tactical Data System Link 4A. The alignment data consist of the aircraft carrier's velocity, attitude, position, and aircraft waypoints in an unencrypted format. Accurate, continuous reference initialization data from SINS are prerequisites for aircraft

carrier alignment, since the navigation accuracy of the aircraft navigation system is dependent on the quality of its initial alignment. Only one SINS is currently installed on each aircraft carrier. If it fails, INS carrier alignment and system maintenance and calibration cannot be accomplished. The SINS system is of mid 1960's vintage and is a major reliability problem.

The operational accuracy and availability of the INS is dependent upon the interface with the ship's SINS and the digital data link. The importance of the ship's reference system cannot be overemphasized. Without a significant improvement in the availability, quality and accuracy of the SINS and the digital data link interface, any improvement to the INS system, hardware and software, would be severely constrained. Effective solutions and improvements to the carrier alignment problem must consider the total INS operational scenario, including the SINS and the interface with the ship's reference system.

After initialization, airborne navigation degrades with time, due to system error sources such as gyro random drifts and uncompensated accelerometer errors. The growth of these errors can be controlled in a highly effective manner using the self-contained Kalman filter software and external measurements of velocity made by a doppler radar or correlation velocity sensor and position fixes made by OMEGA, TACAN, radar, GPS, or JTIDS. Systems that consist of an INS aided by an auxiliary sensor to measure velocity or position are called hybrid navigation systems.

The inertial navigation system installed in the F-14A, S-3A, US-3A, E-2C, A-6E, TC-4C, and RF-4B aircraft is the AN/ASN-92 Carrier Aircraft Inertial Navigation System (CAINS). Previously the A-6A/E and RF-4B, respectively, had the AN/ASN-31 and the AN/ASN-56/74 installed. These systems were replaced with the AN/ASN-92. These aircraft all use the standard Navy Kalman filter alignment software program, called the Single Mode Alignment (SMAL), which was developed especially to cope with the extremely complex problem of initializing an INS on a moving base (aircraft carrier).

The land based naval aircraft have had systems such as the AN/ASN-42 and AN/ASN-84 installed in the past. Starting in 1970 the Navy land based aircraft such as P-3 and C-130 began to be equipped with ARINC-561 Commercial INS that were competitively procured. AN/ASN-42 should be out of the inventory by 1982 while AN/ASN-84 may be kept through 1985.

The A-7E and FMS versions of A-4 utilize the AN/ASN-90. The A-7 system uses the AN/ASN-91 computer to perform the INS navigation compilation while A-4 models use Lear Siegler computer/interface.

Many Navy aircraft, particularly rotary wing aircraft, are not equipped with an INS. These aircraft will usually have an Attitude Heading Reference System (AHRS), a doppler radar, and a dead reckoning navigation computer. AHRS/doppler systems are radiating systems and provide considerably less accurate navigation information than hybrid systems that employ an aided INS.

6.2.1.2 Current Capabilities and Identified Deficiencies

The AN/ASN-92 system was developed in the late 1960s to meet the navigation requirements of the new and updated generation of carrier based aircraft: E-2C, F-14A, S-3A, A-6E, and RF-4B. At the time, a major effort was expended to standardize the INS system among the various aircraft. The technology of the 1960s did not allow complete commonality/standardization of Weapons Replaceable Assemblies (WRAs). The AN/ASN-92 was defined to interface with non-standard aircraft hardware. Consequently, of the five CAINS WRAs used in the E-2C, only two are used in the F-14 and A-6E, and three in the S-3A. The major benefit of the AN/ASN-92 standardization approach has been that the wide system application dictated intense management control which ultimately resulted in the development of a system with high accuracy and, by 1970 standards, good reliability.

The Mean Time Between Failure (MTBF) of the AN/ASN-92 has achieved an acceptable level, but the system Mean Time Between Removal (MTBR) is not improving, due mainly to WRA interface complexity. This is the area that has direct impact on the AN/ASN-92 Not Operationally Ready-Supply (NORS) status of aircraft, since a spare must be available to replace the removed unit. The requirement to calibrate periodically the gyros in the AN/ASN-92 also has a serious impact on system availability. All of these aspects, MTBR, no-defect rate (A799) (a system that is reported to be defective by the aircrew, removed, tested, and found to be fully operational and to have no defect is returned marked A799), and calibration, in addition to the gimbal/gyro design configuration, add a substantial burden to system life cycle cost (LCC).

At the present time, the interface with the carrier (SINS and data link) is the weakest link in achieving rapid and repeatable alignment. No substantial improvement in the AN/ASN-92 operational system (hardware and software) can be achieved without the optimization of this interface. An effective solution and/or improvement to CAINS system problems then must also address aircraft operational flight program software single mode alignment (SMAL), the ship's reference system (SINS) and the data link interface message format as described in AR-57A.

The AN/ASN-92 software is the most sophisticated of its type, since it must provide for the automatic alignment of an INS on an aircraft carrier in the shortest possible time. The development of the Single Mode Alignment (SMAL) software was predicated upon the availability of an optimum interface between SINS and the AN/ASN-92. However, the design of the data link message was oriented toward earlier generations of INS software (least squares fit); no consideration was given to certain fundamental requirements of SMAL or other optimal alignment mechanizations which employ sampled data methods. Consequently, AN/ASN-92/SMAL operational software must use a data link format that is unsuitable for an optimum Kalman filter. Because of this format, SMAL and other optimal alignment mechanizations must pay a penalty in alignment time, the size of the computer program, and, hence, software reliability. It is essential to modify the data link format to satisfy the present and future requirements of carrier alignment software.

The operation of AN/ASN-92 on aircraft carriers depends exclusively on the availability and quality of SINS. In the existing configuration, all AN/ASN-92 equipped aircraft must place total reliance on one single alignment

reference source, that is, SINS. If for any reason, SINS is not working, or even in the process of being aligned, the AN/ASN-92 data link alignment mode cannot be used. This means that most aircraft, e.g., F-14A, must be launched without an alignment and use the AN/ASN-92 in the Attitude Heading Reference System (AHRS) mode. In addition, the lack of valid SINS reference data also makes the Aircraft Intermediate Maintenance Department (AIMD) shop inoperative for the calibration of IMU's.

The present operation of the AN/ASN-92 on an aircraft carrier is adversely affected by two distinct problems related to the ship interface:

* Use of cables during emission control conditions (EMCON).

* Inadequate alignment information on the data link.

The use of umbilical cables for aircraft INS alignment on aircraft carriers is due to the use of Link 4A to receive alignment and waypoint information. Link 4A is a non-secure link and under EMCON conditions must be shutdown, requiring the aircraft to use umbilical cables. This creates the following problems:

* Cumbersome (long and heavy) cables create hazards that complicate normal flight deck procedures.

* Aircraft must be spotted within 115 feet of the Alignment Outlet Box (AOB) so that the umbilical cable can reach the box. There are a limited number of AOB's on the flight deck.

* Aircraft cannot be moved during the course of the alignment while the umbilical cable is connected.

The alignment data included in the present data link are affected by the following deficiencies:

* The parameters transmitted are not in a form suitable to AN/ASN-92 software.

* Most of the parameters required by the optimal Kalman filter, which should be generated in the SINS computer, must be generated in the CAINS computer.

* No growth potential is available to transmit other important aircraft data, such as additional waypoints and mission parameters.

The SINS data link format should be changed. This will permit a significant simplification in the existing AN/ASN-92 filter software and will provide additional capability to present and future generations of CAINS, such as CAINS II.

Particular missions of non-inertially equipped aircraft require inertial systems. Palletized ARINC-561 systems have been procured for this use. These systems, however, can not be operated from aircraft carriers and palletized CAINS systems need to be procured for this purpose.

The objectives in Naval air navigation should include efforts to solve the aforementioned navigation problems. Efforts related to the enhancement of hardware currently operational in Navy aircraft, and the development of new systems to satisfy the interface requirements of new or CILOP aircraft that include MIL-STD-1553 MUX bus interfaces, are presented below.

6.2.1.3 Equipment Development and Modernization

The following paragraphs describe the current status and requirements in the short, mid and long term time periods for the AN/ASN-92 (CAINS I), AN/ASN-130 (CAINS IA), CAINS II Development, Strapdown INS, CAINS/SMAL Improvement Program, EHF Digital Data Link, CAINS/OMEGA Integration, CAINS/GPS Integration, and the CAINS Reference System.

CAINS AN/ASN-92 (CAINS I)

The CAINS AN/ASN-92 (CAINS I) is the most widely used INS in Navy aircraft. The AN/ASN-92 production line was started in 1972 and will continue through the 1983 time frame. Its usage on the Navy's first-line tactical aircraft (F-14A, A-6E, S-3A, E-2C and RF-4B) makes its availability critical. The Navy will have approximately 1400 AN/ASN-92 systems in its inventory, which are to be utilized into 1990 and beyond by all Navy carrier based aircraft prior to CILOP.

A CAINS reliability improvement program was initiated by NAVAIR to investigate and develop cost effective AN/ASN-92 reliability improvements. NAVAIR has established a five-year maintenance contract based on a Reliability Improvement Warranty (RIW). This program, identified as CAINS Reliability and Operational Warranty for the Navy (CROWN) is specifically designed to improve the operational availability of the AN/ASN-92. The AN/ASN-92 system will continue to satisfy the Navy requirements prior to aircraft CILOP and, at the same time, can be utilized as a standard ship system for the development of CAINS Reference System (CRS) for various Navy ships navigation needs.

Summary of Requirements for AN/ASN-92

Short Term (0 to 5 years) -

* Effective implementation and support of CROWN.

* Assessment of CROWN support approach to determine if the Navy should establish an organic support for subsequent years and, if so, identify necessary actions and related timetables.

* Design and test of a navigation computer to replace the AN/ASN-92 Airborne Navigation Computer Unit (ANCU) in the E-2C, S-3A and RF-4B. The ANCU is affected by memory alterations and poor reliability.

* Development and test of a motor generator or a state-of-the-art battery to replace the existing Nickel-Cadmium battery pack in the AN/ASN-92 Power Supply Unit (PSU). In addition, the back-up power is required for use with future INS systems for application in aircraft without a battery.

* Procure the required hardware to install the CAINS Reference System (CRS) in the AIMD Shop of all aircraft carriers to support AN/ASN-92 alignment/calibration prior to the Fleet introduction of the dual MINISINS (DMINS).

Mid Term (5 to 10 years) -

* Continue support for all CAINS equipped aircraft.

* Fleet introduction of a navigation computer to replace the CAINS ANCU in E-2C, S-3A, and RF-4B aircraft.

* Replace the nickel-cadmium battery of AN/ASN-92 PSU with either a motor generator or new state-of-the-art battery pack.

* Initiate replacement of AN/ASN-92 with CAINS II in CILOP aircraft.

Long Term (10 years plus) -

* Continue support for those aircraft that are not updated.

* CAINS II operational in lieu of AN/ASN-92 in F-14A, S-3A, A-6E and E-2C.

* AN/ASN-92 inertial measurement unit to be widely used with a separate computer as a CRS in most Navy ships.

CAINS AN/ASN-130 (CAINS IA) for F-18

The AN/ASN-130 (CAINS IA), designed to satisfy the functions and requirements of the F-18 aircraft, is now in the early stages of production. The CAINS 1A includes a MIL-STD-1553 MUX bus and a new generation of inertial sensor, utilizing a dry gyro rather than a floated gyro. The inertial sensor is identical to the ARINC-561 (LTN-72 version). Like its predecessor, the AN/ASN-92, it retains the conventional and complex electromechanical gimbal assembly and mechanically rotating gyros that require periodic calibration to compensate for drift rates. Both of these aspects of a gimballed INS add substantially to the system LCC. However, the core memory is being replaced by ultraviolet Erasable Programmable Read Only Memory (EPROM) to reduce the LCC. The F-18 will continue to utilize the AN/ASN-130 until the follow-on CAINS II has been granted Approval for Service Use (ASU). Since the CAINS II will be AN/ASN-130 compatible, the F-18 could then use the CAINS II and obtain the inherent LCC advantage.

Summary of Requirements for AN/ASN-130 (CAINS IA)

Short Term (0 to 5 years) -

* Begin production of AN/ASN-130 INS for the F-18.

* Fly-off comparison with McDonnell Douglas Corporation/Honeywell RLG in AV-8B.

* Change F-18 INS from Contractor Furnished Equipment (CFE) to Government Furnished Equipment (GFE).

* Conduct a LCC study to compare the AN/ASN-130 vs. CAINS II systems.

* Deliver GFE SMAL tape to Fleet prior to first deployment of F-18.

Mid Term (5 to 10 years) -

* As a result of CROWN, assess the option of subsequent contract or organic support for the AN/ASN-130. Formulate the most effective support structure.

* Continue GFE procurement of the AN/ASN-130.

Long Term (10 years plus) -

* Continue support of the AN/ASN-130. If a mix of AN/ASN-130 and CAINS II is available in Navy inventory, allocate hardware to minimize the impact on logistics.

CAINS II Development

The development of CAINS II will provide the Navy with a new generation of standard INS, and yet retain compatability with the standard CAINS I and IA Ground Support Equipment. The CAINS II will be the natural replacement for the AN/ASN-92 in all CILOP aircraft and the primary candidate for forward fit into new aircraft. The CAINS II will be designed to be AN/ASN-130 compatible and will include Ring Laser Gyros (RLGs) mounted in a strapdown configuration. This eliminates the complex and costly electromechanical gimbal arrangement. Advanced development models of an RLG INS have demonstrated acceptable navigation accuracy and have gyros that possess long term bias characteristics that should remain stable throughout a carrier deployment without requiring recalibration. This stable bias characteristic may solve a major INS logistic support problem by making it possible to eliminate the intermediate maintenance level shipboard gyro biasing equipment now installed aboard aircraft carriers.

The CAINS II design approach is a single box INS with a MIL-STD-1553 MUX interface. The CAINS II computer will include solid state memory to eliminate the core memory alteration problems being experienced by current systems. In addition, CAINS II will use distributed microprocessors dedicated to partitioned software functions to simplify software development and support and ensure that the system computational capability will satisfy future aircraft Input/Output (I/O) function requirements. The CAINS II computer system will also include a stored standard magnetic variation look-up table and pertinent INS "life history" (i.e., system serial number, date of last calibration, BIT retention, etc.) that can be used in conjuction with the ground support equipment (GSE) AN/ASM-608 to ascertain the status of the system and minimize the AN/ASM-608 test time. The CAINS II will use military qualified microprocessors with established second sources. The CAINS II development program will concentrate on achieving the following system characteristics:

* Increased system availability, by using an INS based on RLG strapdown technology.

* Simplified software development and support.

* Complete compatibility with AN/ASN-130 to ensure that CAINS 1A can be directly replaced by CAINS II.

* Improved reliability and maintainability through the use of a single WRA INS.

* Continued improvement of AN/ASM-608 as programmable GSE for testing WRA's and SRA's.

* Increased system Mean Flight Hours Between Repair (MFHBR) time.

* Reduced total system LCC.

* Compatibility with advanced avionic system architectures through the use of a MIL-STD-1553 multiplex data bus.

It is important to point out that the CAINS II offers the Navy an opportunity to establish a competitive scenario for procurement in future Navy acquisition of INS. Several contractors have made major investments and commitments for RLG INS production. Unless the CAINS II program is reality, the AN/ASN-130 system will be "sole-source" for future Navy INS acquisitions.

The CAINS II inertial navigation system developments include the following:

* Drastic system simplification and reduction in LCC through the use of RLGs in a strapdown INS.

* Use of dedicated microprocessors to perform partitioned computations (e.g., coordinate conversion, Kalman filter, navigation).

* Provide the capability to accept and process any reference data available on the MUX bus, such as position data from OMEGA and the GPS satellite system.

CAINS II is a planned Full Scale Engineering Development program (Category 6.4) scheduled to commence in FY-83. Preliminary system definition and acquisition planning are being supported by the Advanced Technology Demonstration (ATD) Laser Gyro Project, Program Element 63202N.

Major milestones (0-2 years) under the ATD project phase are:

FY 81	Complete system specification
FY 82	Complete acquisition planning

Summary of Additional Requirements for CAINS II Development

Short Term (0 to 5 years) -

* Complete procurement phase of CAINS II.

* Complete contract phase with initial hardware delivery.

* Complete development of GSE hardware.

* Initial phase of Navy test and evaluation.

Mid Term (5 to 10 years) -

* Complete Navy test and evaluation.

* Obtain Approval for Service Use (ASU).

* Begin retrofit and forward fit of CAINS II into CILOP aircraft and new aircraft.

* Prepare a comprehensive plan for the disposition and utilization of AN/ASN-92 hardware made available from CILOP aircraft (CRS, spares, etc.).

Long Term (10 years plus) -

* Continue retrofit and forward fit of CAINS II.

Strapdown INS: At-Sea and In-Flight Alignment Tests

(These tests are designed to define the baseline for the CAINS II program development.) A CAINS compatible RLG Inertial Measurement Unit (IMU) and an ADM ring laser gyro navigator (RLGN) have been tested extensively by the Navy to establish the feasibility and potential of the RLG strapdown technology. Flight tests were carried out on F-14A, A-7E, and P-3C aircraft and a preliminary at-sea test was conducted. However, additional tests are required to assess the capability and potential of the strapdown technology for CAINS application.

The SMAL program was developed for the AN/ASN-92. With the development of a strapdown inertial system, such as CAINS II, SMAL will require modification and optimization for use in alignment of a strapdown INS. The SMAL software of the E-2C/CAINS was modified to assess the feasibility of a strapdown RLG IMU form, fit, function replacement for the CAINS IMU. Preliminary data on RLG carrier alignment capability were obtained, primarily under straight steaming conditions. Further work must be done to develop an optimal strapdown INS at-sea alignment capability. The alignment software should be extensively tested at sea under a full range of operating conditions.

Another approach to the limitations of carrier alignment is to perform in-air alignments. The feasibility of rapid and accurate alignment of a strapdown INS in-flight must be investigated for a variety of position and velocity references; e.g., air data, doppler radar, GPS, JTIDS, OMEGA, and

Synthetic Aperture Radar (SAR). Those INS/reference hybrid combinations which demonstrate the greatest potential improvement should be implemented in the Navy standard SMAL software in CAINS II.

Summary of Requirements for Strapdown INS

Short Term (0 to 5 years) -

* Continue development of an optimal at-sea alignment capability for a strapdown INS.

* Conduct carrier at-sea alignment tests to define SMAL for strapdown application.

* Develop in-flight alignment algorithms utilizing air data, Omega, doppler radar, GPS, JTIDS, SAR, or other potential alignment references.

* Conduct flight tests of in-flight alignment algorithms.

* Define SMAL algorithms for the most promising techniques.

Mid Term (5 to 10 years) -

* Implement carrier alignment and in-flight align features into CAINS II system.

Long Term (10 years plus) -

* Monitor and optimize software to improve system performance and capabilities.

Programs

* Research and Technology AIR-360
  Program Element Number: 63202N
  Title: ADM Program RLG At-Sea Alignment

  - Major milestones:

FY 81	Formulate Filter
FY 82	Design filter and integrate with RLGN program
FY 83	Verify in laboratory and initiate sea tests
FY 84	Complete sea test and do analysis
FY 85	Issue report and formulate filter for Fleet usage

* Systems and Engineering AIR-05
  Title: CAINS Program RLG At-Sea and In-Flight Alignment

  Program initiated in FY-77 under CAINS Reliability Improvement Program (CRIP). Accomplishments to date: (a) SMAL/RLG filter definition and implementation into CAINS operational software (FY-78); (b) laboratory tests, flight test on F-14A aircraft, and

preliminary at-sea alignment tests (FY-79); (c) evaluation and analysis of data, preparation and publishment of test results (FY-80).

- Major milestones (Planned):
  - FY 81 Conduct in-air alignment tests and complete carrier tests of RLG/SMAL
  - FY 82 Optimize SMAL/RLG software for the definition of standard CAINS II software

* Systems and Engineering AIR-05
Title: CAINS/Air data integration for in-flight align (Planned)

- Major milestones:
  - FY 81 Collect data on air data to define error model and implement changes into E-2C/CAINS/SMAL. Conduct flight tests to assess feasibility of CAINS in-flight align using air data
  - FY 82 Evaluation of data to determine feasibility of approach and incorporation into operational software

* Research and Technology AIR-360
Program Element Number: 61152N
Title: SAR Velocity Application

- Major milestones:
  - FY 81 Perform feasibility study

CAINS/SMAL Software Improvement Program

The major objectives of this program are (a) to enhance the operational reliability of the SMAL software and (b) to optimize SMAL software in order to reduce the aircraft down time under all operational conditions. The enhancement of the operational reliability of the CAINS software is predicated on a corresponding upgrading in the interface between CAINS and SINS. There are several known problems associated with the processing of SINS reference data and the data link interface between SINS and CAINS. These problems are related to the SINS processing of the reference alignment parameters and the data link message design.

Any improvement in the CAINS software will be severely constrained unless the CAINS/SINS interface is redesigned in terms of present and future requirements of CAINS.

The optimization of CAINS operational software consists of three distinct facets of improvement: (a) SINS processing of reference alignment data, (b) general SMAL software, and (c) data link format.

Summary of Requirements for CAINS/SMAL Improvement Program

Short Term (0 to 5 years) -

* Study, evaluate and analyze the SINS processing of the reference alignment parameters used by the CAINS.

* Conduct an at-sea test to monitor and assess short term SINS performance using the CRS as a reference. Evaluate data to determine any potential problem.

* Implement the proposed changes to the CAINS/SMAL operational software.

* Implement the MK 19 gyrocompass/EM Log back-up alignment mode to supplement SINS reference.

* Conduct carrier tests to assess operational advantages of proposed CAINS/SMAL enhancements.

Mid Term (5 to 10 years) -

* Continue to analyze test data and finalize formulation of software for CAINS II development/support.

Long Term (10 years plus) -

* Continue to test, identify potential problem areas and improve CAINS operational software/hardware.

SINS Data Link Format Improvement

This section presents the approach for the implementation of an optimum input signal and data processing method for the Single Mode Alignment (SMAL). The signals are generated by the computer of the SINS (or the CRS), and are transmitted by a digital data link to the aircraft's computer, where the SMAL Kalman filter is mechanized to perform the alignment. The optimum signal design was developed within constraints imposed by existing carrier reference systems (SINS or CRS) and data link equipment and is compatible with SMAL and any other class of discrete digital alignment filters.

The primary objective of the proposed changes is to define an optimum data link format that satisfies present and future requirements of Kalman filter alignment aboard aircraft carriers. The proposed modifications to the alignment data formats transmitted from the SINS or CRS to the CAINS are designed to provide the following fundamental improvements to the existing format described in AR-57A:

* Provide faster alignment capability.

* Provide time-synchronized data sets at a 4 Hz rate.

* Provide continuous integrals of SINS velocity to prevent loss of data during periods of transmission interruption.

* Add SINS mode information to the message.

* Add Greenwich Mean Time and Julian date to the message.

* Add dead-reckoning reference data to the message for back-up alignment capability.

* Provide both alignment and waypoint data on a single data link channel. Both channels can be used to transmit the same data redundancy.

* Provide for additional waypoint and mission parameters not currently transmitted.

* Adjust scaling and formats of some data for better compatibility with CAINS software.

* Eliminate unused items from the current message.

Summary of Requirements for the CAINS/SMAL Improvement Program

Short Term (0 to 5 years) -

* Define a Universal Carrier Data Link (UCDL) format that would satisfy present and future CAINS interface requirements.

* Amend AR-57A to include the modified format.

* Implement the UCDL format into the MK 3 MOD 7 SINS and/or DMINS and CRS.

* Modify CAINS/SMAL software to accept and process the modified format. Conduct carrier tests to verify system operation enhancement.

Mid Term (5 to 10 years) -

* Implementation of modified data link format into the CAINS/SMAL operational software of all CAINS equipped aircraft.

Extremely High Frequency (EHF) Digital Data Link

An EHF receiver is proposed for use in lieu of the current Ultra High Frequency (UHF) receiver for the Radio Frequency (RF) data transfer associated with CAINS alignment and waypoint insertion. The EHF data link transmits at a 60 GHz frequency which the atmosphere conveniently absorbs, thus limiting its detection range to less than 2000 ft. This is a covert link that could be used during EMCON conditions. Although future data links such as JTIDS may be secure they will be detectable, thus preventing their use during EMCON conditions. The EHF receiver will be an add-on equipment that receives the RF information from the ship's transmitter, demodulates the signal and provides a digital output to the digital data link equipment (AN/ASW-25 or AN/ASW-27). An EHF antenna will be located in the aircraft to provide line-of-sight (LOS) to the ship's transmitter antenna. (The French have developed and deployed on their carriers a possible competitor to the EHF system that uses an infrared signal between the ship and the aircraft.)

Use of EHF has been demonstrated in applications other than CAINS alignment that require short-range secure communications. Much progress has been made in EHF development since it was last considered in 1969 for CAINS data transmission. It is now possible to build EHF receivers and antennas that are extremely small, lightweight and reliable. The EHF receiver and transmitter units will each be approximately 2 x 3 x 5 inches and weigh between two and three pounds.

Summary of Requirements for the EHF Digital Data Link

Short Term (0 to 5 years) -

* Develop a prototype EHF transmitter/receiver.

* Conduct actual carrier tests to validate the technical approach.

* Conduct carrier tests with the French-developed infrared system.

* Formulate a program plan for the retrofit of the EHF in all CAINS equipped aircraft of the better and less expensive system.

Mid Term (5 to 10 years) -

* EHF or infrared data link operational in all CAINS equipped aircraft.

Long Term (10 years plus) -

* Utilization of 60 GHz or infrared data link transmission to load Cruise Missile Tactical Program.

CAINS/OMEGA Integration

The OMEGA is an all-weather very low frequency (VLF) radio navigation system, which uses eight strategically located transmission stations around the world. The interest in the OMEGA system in both military and commercial sectors of aviation is mainly due to its low cost and acceptable position accuracy. The Navy developed the original OMEGA receiver, the AN/ARN-99, which has a limited military application in P-3C aircraft and ships. The limited utilization of the AN/ARN-99 is mainly due to its high cost and weight. However, the Navy has recently begun the procurement of the commercial OMEGA system (the LTN-211), a state-of-the-art unit that provides substantial reduction in cost and weight. In most applications, the OMEGA system is ideally suited to bound the CAINS position error propagation and to perform in-flight alignment. In some cases, the OMEGA could be used to replace old and unreliable equipment (e.g. the AN/APN-153 doppler radar in the E-2C). However, the OMEGA needs to be integrated with CAINS. The objective of this program is to integrate the OMEGA system (LTN-211) with the CAINS, define hardware and software interfaces and conduct a flight test to determine the advantages of the integration approach. The CAINS/SMAL software of the E-2C aircraft will be modified to incorporate the appropriate error models and to process the OMEGA navigation data. An interface between the OMEGA system and the CAINS LC-728 computer must be designed and built. The integration of

CAINS with external navigation aids such as OMEGA will enhance system capabilities and reduce system LCC. The collateral result of this test is the definition of the SMAL filter to process the OMEGA navigation data. The SMAL/OMEGA software would then be implemented into the CAINS II program.

Summary of Requirements for the CAINS/OMEGA Integration

Short Term (5 to 10 years) -

* Design interface between CAINS ANCU and LTN-211 OMEGA system.

* Modify SMAL software to accept and process OMEGA signals.

* Conduct flight tests to determine the advantages of an integrated CAINS/OMEGA System. Extrapolate results for applications with AHRS/OMEGA.

Mid Term (5 to 10 years) -

* If test results indicate a specific CAINS/OMEGA advantage, implement SMAL/OMEGA into appropriate CAINS equipped aircraft.

* Perform comparable integration with AHRS equipped aircraft.

Long Term (10 years plus) -

* Continue to support and improve CAINS/OMEGA and AHRS integrations.

Program

* Systems and Engineering AIR-05
  Title: CAINS/SMAL/OMEGA Integration (Planned)

  - Major milestones:

FY 81	Design and build interface between LTN-211 Omega receiver and LC-728 CAINS computer
FY 82	Modify CAINS/SMAL software to process Omega inputs. Conduct laboratory and flight tests
FY 83	Make CAINS/SMAL/OMEGA available for Fleet application

CAINS/GPS Integration

The AN/ASN-92 CAINS system is the most widely used INS in the Navy inventory. In the present configuration, the CAINS is used mainly in the unaided mode (free inertial). Some CAINS equipped aircraft (e.g. the S-3A) include integration with the doppler radar to provide in-flight alignment and doppler-inertial modes of operation. However, with the advent of the GPS, the integration of INS and GPS would permit position aiding in addition to velocity aiding. The integrated CAINS/GPS can be used not only to provide in-flight alignment capability but also to provide continuous INS system calibration. To accomplish this objective, the GPS must be integrated with the CAINS hardware. Further development of software algorithms is required to

automatically accept, evaluate, and process GPS navigation parameters. A flight test program will be conducted to establish the advantages of an integrated CAINS/GPS. The end result of this development will be the definition of GPS/SMAL software, which can be implemented into the CAINS II system.

Summary of Requirements for CAINS/GPS Integration

Short Term (0 to 5 years) -

* Design optimum interface between GPS receiver and an INS computer.

* Continue development of software algorithms to accept and process GPS parameters.

* Conduct an initial flight test utilizing the strapdown INS to determine an optimum integration approach.

Mid Term (5 to 10 years) -

* Conduct complete flight tests of CAINS INS/GPS, with the full complement of GPS constellations.

* Optimize CAINS/SMAL software for GPS integration.

* Implement SMAL/GPS into CAINS II program.

Long Term (10 years plus) -

* Continue to support and improve CAINS INS/GPS.

Programs

* Research and Technology AIR-360
  Program Element Number: 62721N
  Title: In-Air Alignment GPS/INS and JTIDS/INS Filter

  - Major milestones:
    - FY 81 Publish report on simulation; initiate filter design
    - FY 82 Complete filter design; integrate into ADM RLGN software
    - FY 83 Verify in laboratory - initiate flight tests
    - FY 84 Complete flight tests and initiate report
    - FY 85 Publish report and formulate filter for Fleet usage

* Systems and Engineering AIR-05
  Title: CAINS Program Support (Planned)

  - Major milestones:
    - FY 81 Define processing of GPS data for SMAL filter
    - FY 82 Implementation of GPS processing into CAINS/SMAL software

	FY 83	Conduct CAINS/GPS laboratory tests and flight tests
	FY 84	Data evaluation and filter optimization of SMAL/GPS
	FY 85	Release CAINS/GPS/SMAL tape for Fleet usage

* PMA240 P-3 Project Manager
Program Element Number: 64728N
Title: P-3C/GPS Integration

- Major milestones:

FY 81	Perform simulations and formulate hybrid filters (LTN-72/GPS, LTN-72/Doppler, GPS/Doppler, GPS/Baro Altimeter)
FY 82	Code and integrate filters into CP-901
FY 83	Fly test in P-3C

CAINS Reference System (CRS)

The operation of aircraft INSs on carriers depends exclusively on the availability and quality of the SINS. In the existing carrier configuration, all CAINS equipped aircraft must place total reliance on a single alignment reference source: The SINS. If, for any reason, SINS is not operating, the CAINS data link alignment cannot be performed. In addition, the lack of SINS reference makes the AIMD shop unable to calibrate IMUs, and may also prevent the execution of any at-sea test that may be concurrently taking place to develop, test, evaluate and validate carrier alignment softwares. In the past several critical at-sea tests had to be postponed and/or repeated because of poor or lack of SINS availability on the CV. The delay had some impact on system development schedule and cost.

In the present CAINS/carrier interface configuration, marginal performance of SINS cannot be readily detected, but it results in poor CAINS navigation. This factor is a major contributor to A799's (i.e., CAINS flight components reported inoperative by the squadron, are returned to the AIMD shop for repair, and then returned to the squadrons marked A799, no detectable failure). To remedy this situation, NAVSEA has procured the Dual MINISINS (DMINS) for installation on all carriers. The installation will begin in the 1985 time period.

There is also a requirement to have a SINS type of reference on smaller ships to support the AV-8B, helicopters that will eventually have an INS instead of an AHRS, and VSTOL aircraft. The CRS was proven operationally comparable to SINS to support CAINS aircraft during the at-sea test period on the USS Nimitz in Aug 1980.

The major objective of the CRS program was to develop, as a test tool, a very cost effective alternative to SINS to provide the required ship alignment/navigation reference data for the CAINS Software Support Activity (SSA) instrumentation van for the support and maintenance of the CAINS operational software. The same CRS system could also be used to provide a self-contained carrier reference system to support INS systems on other ships that do not have a SINS installation.

The present CRS mechanization does not include the direct processing of satellite data. It can only accept manual position fixes. The CRS software requires expansion to include interface with TRANSIT, OMEGA and GPS. The CRS is designed to use AN/ASN-92 components, and will make a highly cost effective use of these systems as they are replaced in aircraft by the AN/ASN-130 and/or by CAINS II.

Summary of Requirements for CRS

Short Term (0 to 5 years) -

* Acquisition of the required aircraft WRAs and interfaces to develop necessary numbers of CRS for installation in the AIMD Shop of all aircraft carriers.

* Development of the necessary documentation for the installation and support of CRS.

* Development of software to interface CRS with TRANSIT and OMEGA systems.

Mid Term (5 to 10 years) -

* Development of software to interface CRS with GPS.

* Installation of CRS on ships that do not have SINS.

Long Term (10 years plus) -

* Continue installation and support of CRS as necessary.

6.2.1.4 Development Priorities

The development of the CAINS II system to provide the Navy with an excellent second generation navigation system for use with carrier based aircraft.

The CAINS Reference System is probably the earliest available device that would help to resolve the CAINS-ship interface problem.

The development of CAINS in-flight alignment capability using OMEGA and air data will also help alleviate the problems associated with carrier alignment.

6.2.2 JOINT TACTICAL INFORMATION DISTRIBUTION SYSTEM (JTIDS) RELATIVE NAVIGATION

6.2.2.1 Background

JTIDS Relative Navigation is an outgrowth of the Integrated Tactical Navigation System (ITNS) Program which was conducted in the early 1970s. This program demonstrated the basic technical feasibility of using a distributed

optimal data processing system to derive a very precise coherent navigation grid. It also demonstrated the utility of a relative navigation grid in accomplishing a variety of Naval missions.

With the advent of the JTIDS program in 1975, the relative navigation function of ITNS was further developed in Advanced Development Model (ADM) JTIDS terminals using Time Division Multiple Access (TDMA) (Phase I) and Distributed-TDMA (DTDMA) (Phase II). These efforts resulted in delivery of TDMA terminals in FY 79 and DTDMA terminals in FY 80. As an ADM development, the relative navigation function of these terminals was limited to those capabilities required for test and evaluation.

During the past two years, test and evaluation of the Phase I ADM JTIDS terminals was conducted to support identification of the requirements for the Full Scale Development (FSD) terminals. Although these tests were highly successful, some problems were reported that required further development efforts. Phase II ADM terminals were delivered in FY 80 and tests were initiated; these terminals incorporate the advanced DTDMA communications architecture which has been selected by the Navy for Full Scale Development (FSD).

6.2.2.2 Current Capability and Identified Deficiencies

JTIDS is a jam-resistant, secure communications, navigation and identification system. The proposed JTIDS terminals include the capabilities of digital voice, integral TACAN, and the ability to perform relative navigation, with provision to accommodate multiple message structures. Three generic JTIDS terminal classes have been identified. Class 1 terminals have the highest capability and are intended for use in large ships, and Class 1A terminals are intended for use on airborne early warning aircraft. Class 2 terminals are intended for use on tactical fighter aircraft and surface ship applications requiring less capability than that provided by Class 1 terminals. The Class 3 terminals are the smallest terminals and are intended for applications such as manpack and missile guidance.

JTIDS will provide a precision relative navigation capability with either line-of-sight or extended line-of-sight communications via an airborne relay. The relative navigation capability results from combining precise Time Of Arrival (TOA) data (derived from the JTIDS communications function) with incoming navigation data from other platforms, and navigation data obtained from the onboard navigation system as well. These data are combined in an optimal manner by JTIDS, thus comprising a shared or distributed data processing system.

System laboratory testing is currently in progress on the Phase II ADM terminals. The Phase II JTIDS terminal has also been installed in a large aircraft and is being system tested prior to initiation of relative navigation flight demonstrations.

The ADM Phase I Navy Class 2 terminal, AN/URQ-28 (XN-1), was designed to provide secure, jam-resistant voice and data communications plus TACAN and relative navigation capabilities. The DTDMA ADM Phase II Navy Command Terminal, AN/USQ-72(XJ-1), provides a capability to simultaneously

operate on up to twelve independent nets. It processes voice, digital data, TACAN, and relative navigation, and is interoperable with TDMA. The ADM Phase II DTDMA Navy Tactical Terminal, AN/USQ-75(XJ-1), provides a capability to simultaneously operate on up to four independent nets and processes the same type of data as the Command Terminal. These terminals work with dedicated inertial navigation systems and do not provide operational interfaces with ships and aircraft.

6.2.2.3 Equipment Development and Modernization

The JTIDS system uses and will continue to use two communication technologies developed to satisfy different military service requirements. These two technologies, TDMA and DTDMA, are being developed by the Air Force and Navy, respectively.

A two-stage JTIDS implementation strategy is planned for the Navy. This is necessary because a new message standard, TADIL-J, is not mature, and many shipboard Combat Direction Systems (CDS) are inflexible and incapable of implementing the many new capabilities of JTIDS without major programming and upgrading. The Stage One capabilities that will be developed and implemented for Operational Evaluation (OPEVAL) and Initial Operational Capability (IOC) will provide a significant operational enhancement. The platforms selected for this first Navy operational JTIDS capability are the aircraft carrier and the E-2C and F-14A aircraft. Stage Two implementation will more fully utilize JTIDS system capabilities and will implement the full TADIL-J message standard. Navy development will concentrate on the advanced technology DTDMA but will ensure DTDMA/TDMA interoperability. The relative navigation function of JTIDS will be developed in consonance with the overall JTIDS development. Accordingly, initial FSD efforts will concentrate on the CV, E-2C and F-14A platforms.

Some of the primary technical issues that must be resolved this period are:

* Terminal modularity. The relative navigation function must be implemented as a module to allow functional operability with each of the different host aircraft.

* Contractor-furnished algorithm. The government must increase the level of detail in its development specifications to ensure that the problem areas of performance and integration are solved by the FSD contractor(s).

* Net management. The net management protocol selected must be able to handle any operational situation. Such factors as unfavorable relative placement geometries, varying levels of accuracy of synchronization of net participants, multiple grid environments, etc., must be handled properly.

* Interface coordinates. JTIDS terminals will be installed on a variety of platforms and there must be provision for computing all necessary coordinate transformations.

* Message data requirements. It is desired to make relative navigation no more dependent on data exchange than it is now. Each algorithm change could require changes in the JTIDS messages.

The following are critical performance areas to be solved in generating an acceptable algorithm:

* Successful operation with any mix of fixed and mobile stations.

* Pathological geometries and measurement nonlinearity.

* Long term stability (filter convergence).

* Mode switching - active/passive synchronization switches, changes to and from Navigation Controller status, etc.

* Ship's motion.

* Active synchronization/passive synchronization performance.

* Static geometry (3 or more members of the grid have negligible velocities relative to each other.)

* Accurate navigation quality estimates - failure to solve this problem will result in instability.

* Polar capabilities.

* Undetected grid rotation.

Algorithm options to be considered are the following:

* Active and passive TOA processing - it must be determined whether to process these measurements separately to determine position and synchronization errors, or in a single filter.

* Navigation data source selection - determine best measurements to maintain stability.

* Grid motion modeling - determine best model to estimate grid origin motion.

* Recovery procedures/grid monitoring - must have recovery procedures at both the user level and the community level to be able to deal with any instability which might occur.

* Position update - vehicle self-contained versus community.

* Factorized Kalman filter.

6.2.2.4 Summary of Requirements

Short Term (0 to 5 years) - In 1980 the Navy was directed to proceed alone in the FSD of terminals to satisfy the performance requirements of the JTIDS terminals for Navy and Marine Corps applications. This development will encompass separate enhanced relative navigation algorithms to be developed by each contractor, providing additional capabilities such as target information handling within the relative navigation grid. Advanced techniques will also be implemented to assure optimal performance of the relative navigation distributed data processing function under a wide variety of conditions.

During 1981, design studies will be conducted for FSD leading to the award of FSD terminal contracts. Concurrent with FSD terminal development, relative navigation platform integration efforts will be conducted for the F-14A, E-2C and CV. This is perhaps the most significant problem faced by the JTIDS project. The integration function will be accomplished by the input/output adapter and the platform application group. Integration is a very large effort, and careful planning is now underway.

Mid Term (5 to 10 years) - JTIDS OPEVAL is planned for 1986 with Defense Systems Acquisition Review Council (DSARC) III and Navy IOC in 1987. During this period, the relative navigation function will be expanded to meet all identified requirements of the initial platforms (F-14A, E-2C and CV). The development will be controlled by the Relative Navigation Working Group under sponsorship of PME-109.

Long Term (10 years plus) - Further developments in this period will address the needs of additional platforms selected by the Navy for JTIDS implementation. Developments will also treat new weapons, sensors and combat direction systems as required. It is also expected that development of relative navigation within Class 3 JTIDS terminals will occur in this period.

6.2.2.5 Development Priorities

The essential priorities facing the JTIDS relative navigation community are centered around the following areas:

* ADM relative navigation algorithm enhancement to provide performance required for FSD.

* CV, F-14A and E-2C platform interfacing and systems integration. These efforts will be focused on Class 1, Class 1A and Class 2 JTIDS terminals.

6.2.2.6 Ongoing Programs

JTIDS (P.E. 25604N)

MILESTONES

FSD Contract Award	Nov 81
DTDMA Design Studies	Dec 81
FSD Interface Definition	Jan 82
FSD Critical Design Review	Oct 82

FSD Initial Terminal Delivery	Feb 83
Integration Testing	Jun 85
TECHEVAL	Mar 86

6.2.3 INTEGRATED INERTIAL SENSOR ASSEMBLY (IISA)

6.2.3.1 Background

Military aircraft require inertial sensor data and air data for flight control, navigation, weapons delivery and cockpit displays. These data are presently obtained from a multiplicity of independent onboard reference systems which, while providing necessary data, contribute significantly to the size, weight and costs of the aircraft. These reference systems were developed to satisfy different requirements. The flight control system sensors were required to output body angular rates and body translational accelerations for aircraft stabilization. The flight control outputs are flight critical elements, hence they have a very high safety-of-flight requirement. Therefore the incorporation of redundant sensors and electronics into the flight control system design was a necessity. The navigation function is a mission critical element, hence it does not have the safety-of-flight requirements and did not incorporate redundant sensors or electronics. Historically, the flight control gyros and accelerometers were not of sufficient accuracy for navigation. Likewise, the navigation sensors, while of improved accuracy, were not suitable for flight control, since they were gimballed and did not provide the body axis components of rate and acceleration. Recent technological advances have made available strapdown gyros and accelerometers which inherently provide the body rates and accelerations required for flight control and are of sufficient accuracy for navigation; therefore, the concept of integrating the flight control and navigation functions becomes feasible. This system may become the airborne portion of CAINS II program.

6.2.3.2 Current Capability and Identified Deficiencies

Presently, aircraft systems utilize duplicative sensor assemblies for different functions. This results in a proliferation of equipment, large maintainability costs, reliability problems, high acquisition costs, and weight and volume problems for modern day military aircraft. Utilization of an Integrated Inertial Sensor Assembly (IISA), incorporating laser gyros and linear accelerometers in strapdown assemblies along with support electronics, will provide the needed highly dependable, cost effective source of inertial data while reducing weight and life cycle costs.

6.2.3.3 Equipment Development and Modernization

With the technological advances in laser gyros and digital computers, the Navy has embarked upon an Integrated Inertial Sensor Assembly Program. Major emphasis is on a reduction in the number of sensors required by use of skewed configurations and functional integration. An Advanced Development Model (ADM) IISA will include dual skewed Inertial Sensor Assemblies (ISA), Dual Computer Assemblies (DCA) and a Control Display Unit (CDU). The ISA's will be skewed with respect to each other to further enhance the redundancy information and will include a triad of strapdown ring laser gyros (RLGs) and accelerometers, sensor compensation electronics, and sensor

Built-In-Test (BIT). The dual computer assemblies will each contain two separate but identical processing lines to do the flight control sensor, redundancy management, fault detection, isolation, and navigation algorithms. Critical driving parameters in the system design are the flight-critical, safety-of-flight requirements dictating a fail-op/fail-op/fail-safe (FO/FO/FS) fault tolerance as well as the performance accuracy (1 nm/hr CEP position, 3 ft/sec RMS velocity) necessary for navigation and weapon delivery. Survivability constraints dictate separation of sensor packages and computer assemblies to insure fail-safe flight control operation after a 20 mm hit.

6.2.3.4 Summary of Requirements

Short Term (0 to 5 years) -

* Design, develop, and fabricate an ADM IISA.
* Laboratory test an ADM IISA.
* Perform test bed design activity to define aircraft interfaces, aircraft wiring, and structural modifications and develop the test-bed instrumentation.
* Perform actual aircraft modifications and perform ADM IISA ground tests.
* Perform flight tests and evaluation to demonstrate the key technology issues.

Mid Term (5 to 10 years) -

* Design, develop, and fabricate a full-scale development (FSD) model IISA for a particular aircraft.
* System design will incorporate all of the flight control laws, air data software, and navigation functions and will provide the necessary weapon delivery outputs to the mission computer.
* Installation into a prototype aircraft.
* Ground and flight test evaluation to demonstrate IISA as an integrated system for the use as the flight control electronic set and the navigation system.

Long Term (10 years plus) -

* Installation of IISA into future military aircraft. IISA will be utilized as the flight control system and the navigation system while providing outputs to the mission computer for weapon delivery, cockpit displays, etc.

6.2.3.5 Development Priorities

* Develop an ADM IISA to prove feasibility of a technological concept.

* Develop and demonstrate a FSD IISA for an advanced Navy aircraft.

* Utilization of IISA in advanced Navy aircraft as the primary flight control system and the navigation system.

6.2.3.6 Ongoing Programs

Advanced Technology Demonstration Laser Gyro Project (P.E. 63202N)

MILESTONES

Award Contract	Sep 81
Delivery of ADM IISA	Jun 83
Laboratory and Van Tests Completed	Jun 84
Flight Tests Completed	Sep 85

6.2.4 TACTICAL AIRBORNE NAVIGATION (TACAN)

6.2.4.1 Background

A TACAN system provides distance, bearing and audio identification information indicating the location of a complementary surface station with respect to the aircraft. It also provides distance, bearing and audio identification to other TACAN equipped aircraft. These data are available when operating in a vertically-oriented, cylindrical volume having a radius of 300 miles about the complementary surface station within line-of-sight and up to a height of 70,000 feet above sea level. The AN/ARN-84(V) has the additional capabilities to transmit and receive data link information. Both the AN/ARN-84 and AN/ARN-118 TACAN navigation sets have 126 X-mode channels at 1 MHz spacing. An additional 126 Y-mode channels are provided on the same airborne interrogation frequencies. The AN/ARN-84(V) receiver/transmitter has decoding and data computation capabilities.

The AN/ARN-84, has been used in the Navy since 1972. Since 1978, the Navy has specified the AN/ARN-118, developed by the Air Force, for aircraft requiring its capabilities.

6.2.4.2 Current Capability and Identified Deficiencies

Both systems utilize state-of-the-art integrated circuits; however, vacuum tube technology is used in the power amplifiers in both sets. Although this is not state-of-the-art technology, the performance of the vacuum tube amplifiers is very reliable, having a very high MTBF.

Both the AN/ARN-84(V) and the AN/ARN-118(V) are currently meeting Navy requirements. Deficiencies are relatively minor. The locking nut used to secure the AN/ARN-84(V) in its mounting rack cannot be tightened without injuring the hands of maintenance personnel, especially in cramped quarters. Failure to tighten it causes the unit to vibrate excessively, resulting in frequent intermittent failures in external signal input connectors. A special tool has been developed to secure the locking nuts; this tool should be procured and issued to users.

6.2.4.3 Equipment Development and Modernization

A solid state power amplifier has been developed by an industry source which is plug compatible with both TACAN sets. An investigation should be initiated to evaluate the reliability of the new solid-state power amplifier to determine whether incorporation into the AN/ARN-84(V) and AN/ARN-118(V) TACAN systems is desirable.

6.2.4.4 Summary of Requirements

Short Term (0 to 5 years) - Evaluate the new solid state power amplifier for possible incorporation into the AN/ARN-84(V) and AN/ARN-118(V). The tube power amplifier currently used is highly reliable. Therefore, size, weight, efficiency, and reliability advantages of the solid-state power amplifier must be carefully evaluated.

Mid Term (5 to 10 years) - Consider standardization on a single TACAN system. Investigate the possibility of replacing both TACAN units with JTIDS.

Long Term (10 years plus) - Investigate the impact of Global Positioning System (GPS) on continued use of TACAN in future aircraft. If feasible, replace TACAN units with GPS and/or JTIDS equipment.

6.2.4.5 Development Priorities

First priority should be given to evaluating the possible near term improvement to be gained from use of evaluating the solid state power amplifier.

A second level priority will be the possible elimination of independent TACAN units in favor of integrated systems such as JTIDS and/or GPS.

6.2.5 GLOBAL POSITIONING SYSTEM (GPS)

6.2.5.1 Background

The Navigation Satellite Timing and Ranging (NAVSTAR) Global Positioning System (GPS) is a satellite-based radio positioning and navigation system designed to provide highly accurate three dimensional position and velocity, and time anywhere on or near the earth. Since the early 1960's, both the Navy and Air Force have actively pursued the concept of navigation using radio signals transmitted from satellites. In April 1973, the Air Force was designated the executive service for development of a comprehensive and cohesive satellite navigation system. GPS is a tri-service program managed by the Joint Program Office at the Space Division of the Air Force Systems Command (AFSC). Extensive participation by other services and agencies, including NATO, is being coordinated through their respective Deputy Program Managers. GPS consists of a space segment, a ground control segment, and a user segment. The Navy is responsible for integrating GPS user equipment into Navy and Marine Corps aircraft, and twenty aircraft have been identified by CNO and CMC for installation of hardware in the FY 85-90 time frame.

The Transit navigation satellite system will be supplanted by GPS. With continuous, global coverage provided by the 18 satellites planned, users with onboard GPS receiver systems will be provided precise time and three-dimensional geodetic position and velocity data. The projected accuracies are 16 meters in position and 0.3 knots in velocity under good geometry conditions. The user equipment is passive, and any number of receivers may be in use simultaneously. The system incorporates significant antijam capability. Initial applications for Naval aircraft include the P-3C, EP-3C, S-3A, and E-2C aircraft.

6.2.5.2 Current Capability and Identified Deficiencies

GPS is currently in Full Scale Development (FSD) with a Defense System Acquisition Review Council (DSARC) III (production approval) scheduled for September 1983. Six satellites are presently in orbit and will be retained through the Initial Operational Test and Evaluation (IOT&E) period. User equipment is being developed competitively by two industry sources for evaluation in a variety of air and surface applications including the A-6E, P-3C, F-16, and the UH-60 for the Army. During the FSD phase of the program, the user segment activities will concentrate on design, development and test of user equipment prototypes. The two contractors will develop the basic set architecture for a family of user equipment hardware to be used in all classes of user equipment. The Navy is responsible for integrating GPS user equipment into the A-6E and P-3C IOT&E aircraft.

6.2.5.3 Equipment Development and Modernization

GPS had a highly successful Phase I (Advanced Development). As a result, and as one of the selling points for Congressional approval of the GPS appropriation, the government is projecting cost saving through discontinuance of certain federally supported radio navigation aids, of which TACAN is the principal system utilized by Naval aircraft. This viewpoint at high levels in the government can be expected to produce strong pressure for rapid deployment of GPS, so that the older systems may be discontinued and the savings realized. Also, Phase I testing indicates GPS can be used for non-precise approaches, and probably for precision approaches to any fixed runway. Flight crew demand for this feature can be expected to grow since carrier based aircraft are presently limited to Ground Controlled Approach (GCA) instrument approaches to fixed runways, and the number of airfields with GCA capability is rapidly declining. The Marine Corps will be able to use this approach capability for temporary airfields.

6.2.5.4 Summary of Requirements

Current - The Joint Program Office is focusing exclusively on the development of prototype user equipment and integration into the designated IOT&E platforms.

Short Term (0 to 5 years) - The Program Objectives Memorandum (POM) 82 designates twelve fixed wing and eight rotary wing aircraft types to receive GPS user equipment. These installations must be designed and developed. Also, the following technical areas require development:

* GPS/INS Integration - A GPS receiver performs better if it has an independent measurement of velocity, and inertial navigation systems (INS) perform better with frequent position updates to limit error growth. An integration of GPS and INS functions would improve the performance of both systems. During this period, the GPS/INS hardware interface and the software algorithms within each set (GPS and INS) required to optimally utilize the information provided by the other should be developed.

* GPS/Data Link Integration - GPS provides extremely precise position and time measurement, which will enhance tactical coordination if combined with a suitable data link, such as the Joint Tactical Information Distribution System (JTIDS). Target data transfer, intercepts, and rendezvous can be processed more expeditiously if all participants are operating in a common coordinate frame. JTIDS is a particularly appealing system for GPS integration because of its localized grid navigation and time dissemination capability. JTIDS will benefit from the absolute reference provided by GPS. The mix of JTIDS and GPS equipment to be deployed needs to be determined. Overall aircraft integration cost can be reduced through standardization.

* GPS Guided Standoff Weapons - Although GPS receivers suitable for use in missiles and glide bombs present technical difficulties, they offer a very attractive capability. When target coordinates are determined by a long range or remote sensor, a weapon could be released at a safe distance which would guide itself to the specified coordinates. This would be extremely useful against high value, heavily armed targets such as surface ships. Weapons of sufficient range are already available. A GPS receiver suitable for the weapon and to integrate it with the weapon control system must be developed.

Mid Term (5 to 10 years) - This period will include Initial Operational Capability (IOC) (worldwide two dimensional coverage), Full Operational Capability (FOC) (worldwide three dimensional coverage), and three years of operational use. During this time, the rest of the Navy and Marine Corps aircraft designated to receive GPS will require the design and development of aircraft installations. GPS product improvement will be initiated as operational experience is gained. As GPS becomes widely available, the following developments are anticipated:

* Cooperative Electronics - The extremely precise GPS time allows synchronization of remote platforms to tens of nanoseconds, even beyond line of sight of one another. Electronic equipment can take advantage of this for such things as cooperative Electronic Countermeasures (ECM), controlling transmissions to give a deceptive appearance to the enemy; or cooperative (bistatic) radar, where the transmit and receive functions are separated.

* Tactical Coordination - New tactics will be developed to take advantage of precise common coordinates and common time. New control and display capability and novel operating modes are likely to be required.

* Differential GPS - Even greater accuracy can be achieved in a local area by comparing the outputs of two GPS receivers to determine the separation between them. This would be useful in a situation such as landing a helicopter aboard a ship. This development presumes some form of GPS/data link integration.

Long Term (10 years plus) - In this term older navigation systems will be phased out, requiring development work to manage their removal and to insure no lapses of coverage. GPS product improvement will continue, such as:

* GPS/INS Integrated Receiver - The benefits of INS/GPS integration may be more economically achieved through the development of a GPS receiver which contains a set of inertial sensors. A single set containing inertial components and GPS receiver components is technically feasible, should perform better than two separate systems, and can reduce overall aircraft integration cost through standardization.

* GPS/JTIDS Integrated Receiver - A full integration of the GPS and JTIDS functions within a single set can enhance the benefits of GPS/data link integration described under short term requirements.

* GPS/OMEGA - Where OMEGA is a back-up to GPS in case of denial of GPS.

6.2.5.5 Development Priorities

Deployment of GPS will require an extensive platform integration effort over the next several years. Priority should be given to development of a standard GPS/INS receiver and to GPS/data link integration; this will reduce overall platform integration cost.

GPS will provide worldwide three dimensional navigation to an unlimited number of users. Deployment of GPS will require an extensive avionics retrofit, the cost of which can be reduced if timely standardization techniques are developed. The extreme precision of GPS, including time synchronization, will enhance military effectiveness. Achieving this enhancement will require a continuing development effort.

6.2.5.6 Ongoing Program

NAVSTAR GPS (P.E. 64778N Primary, P.E. 63401N Contributing)

MILESTONES

FY 81	
Initiate Developmental Test and Evaluation	Jul 81
FY 83	
Complete Full Scale Development of GPS User Equipment - DSARC III	Sep 83

FY 84	
Commence Production of GPS User Equipment	Jan 84
FY 85	
Establish Worldwide Two Dimensional Capability	Sep 85
FY 86	
Initiate Deployment in Fleet Aircraft (A-6E and P-3C)	Jan 86
FY 87	
Establish Worldwide Three Dimensional Capability (IOC)	Jul 87

6.2.6 LIGHT AIRBORNE MULTIPURPOSE SYSTEM (LAMPS) MK III NAVIGATION

6.2.6.1 Background

The LAMPS MK III navigation system includes a set of situation sensors, a Navigation Switching Interface Unit (NSIU) and a set of flight critical displays. The situation sensors [Attitude Heading Reference System (AHRS), doppler radar [Radar Navigation Set (RNS)], magnetic compass, TACAN navigation set, radar altimeter, and barometric altimeter] sense the various parameters and send them to the NSIU. The NSIU processes and routes this information to the Flight Critical Displays (FCD). The NSIU calculates: (a) the angular deviation of the aircraft based on the TACAN bearing and Required Course Synchro (RCS) inputs, (b) the required aircraft heading based upon the RCS inputs and the calculated drift measurements, and (c) the estimated ground speed derived from an analysis of the RNS velocity inputs. The NSIU provides routing and switching of; (a) the pitch, roll, and magnetic heading 3-wire synchro data from the AHRS to the attitude direction instruments [attitude indicator (AI)] and the converter-multiplexer (C-MUX), (b) the deviations to the pilot's and the Air Tactical Officer's (ATO) horizontal situation indicators [bearing, distance, heading indicator (BDHI)] as an analog DC signal, (c) the required heading synchro signals to the BDHI's, and (d) the ground speed to the BDHIs via a tri-level ARINC-582 data bus interface. The NSIU outputs a nu...ber of discrete flag signals to the BDHIs based upon the inputted mode select discretes and on the results of data calculations.

The FCDs consist of two identical sets of six instruments. One set each is used by the pilot and the ATO. Each set is composed of one each of the following instruments: AI, BDHI, airspeed indicator, radar altimeter, barometric altimeter, and slip indicator. These instruments are much the same as the corresponding instruments in the LAMPS MK I Seasprite helicopter. These instruments are electro-mechanical devices with dial type pointers. Since the pointers and electrical coils that turn the pointers are small, these instruments are correspondingly delicate.

6.2.6.2 Current Capability and Identified Deficiencies

The failure of the NSIU would make the aircraft incapable of performing its mission. The NSIU was designed in 1969 using discrete components which have been shown to have relatively poor reliability.

Because of the delicate nature of the FCDs, the vibration specification in LAMPS MK III was reduced by 60%. (This was feasible because the vibration environment at the mounting locations was not as severe as originally specified.)

6.2.6.3 Equipment Development and Modernization

Present and proposed military and space aircraft are replacing the FCDs with vertically formatted displays and/or integrating them into a single CRT type display. These newer displays are smaller and lighter, more reliable, consume less power and allow a rapid, more accurate scan by the pilot.

The capability now exists to replace the discrete circuitry in the NSIU with highly reliable LSI circuitry without affecting any aircraft wiring or circuitry.

The incorporation of new algorithms in the present Air Operational Program (AOP), which is resident in the mission computer [AN/AYK-14(V) (XAN-1A)] would permit the calculated navigational commands, which are presently used to drive the displays, to be used as inputs to the Automatic Flight Control System (AFCS). This would permit the pilot to accomplish point-to-point navigation as well as an automatic approach-to-hover through the AFCS using the manual, semi-automatic or fully automatic mode. The net effect would be the addition of a complete Flight Director System (FDS) vice the current partial system. Most present multipilot aircraft such as the P-3, have FDS capabilities.

6.2.6.4 Summary of Requirements

Short Term (0 to 5 years) -

* Replace the FCDs with corresponding vertically formatted units. This would reduce the weight of the aircraft, while allowing a quicker, more accurate, visual scan.

* Replace the NSIU with new modules which utilize highly reliable LSI technology. This will reduce the size, weight, power consumption, and life cycle cost of the unit.

* Incorporate new algorithms in the AOP thus allowing the AN/AYK-14(V)(XAN-1A) to input the calculated navigational commands to the AFCS. This would allow point-to-point navigation as well as approach-to-hover using the AFCS in the manual, semi-automatic, or fully automatic mode.

Mid Term (5 to 10 years) -

* Increase the memory size and power of the NSIU's embedded microprocessor. A faster, more capable microprocessor system will allow further integration of the FCDs with the navigation system.

* Replace the FCDs with a CRT type programmable display. This would give the pilot and ATO a more concise picture of the aircraft situation. Programmability will enhance future system modifications.

Long Term (10 years plus) -

* Add a Heads-Up-Display (HUD) that would allow the pilot to constantly monitor the aircraft situation at all times, while in all types of weather and tactical modes.

* Incorporate the Global Positioning System (GPS) into the navigation system. Coupled with an advanced Inertial Navigation System, (INS), the resultant system will be highly accurate, self contained, lighter, and consume less power.

6.2.6.5 Development Priorities

* Replace the NSIU with modules utilizing LSI technology.

* Add a complete FDS by the incorporation of new algorithms in the AOP.

* Replace the current FCDs with vertically formatted displays.

* Add a HUD system.

* Incorporate a GPS.

6.2.6.6 Ongoing Programs

Advanced Integrated Display System (AIDS) (P.E. 63202N)

MILESTONE

Develop modular system to be utilized in tactical aircraft, anti-submarine warfare aircraft, etc.

Instrumentation (P.E. 62241N)

MILESTONE

Develop color and helmet mounted displays for Fleet.

6.2.7 ATTITUDE HEADING REFERENCE SYSTEM (AHRS)

6.2.7.1 Background

The AN/ASN-50/73, AN/AJB-3, AN/AJB-7, A/A24G-39 and the AN/ASN-116 are currently the Attitude Heading Reference Systems in the Navy inventory. Unfortunately, AHRS have not been considered glamourous in the R&D community so no R&D funding has been forthcoming for over 10 years to develop a new generation of equipment. A major deficiency exists in that there is no AHRS

that is all attitude and no AHRS that is compatible with the MIL-STD-1553 data bus. A further deficiency exists relative to the magnetic azimuth detector. The current sensor was developed over 20 years ago and the need for a solid state detector is well documented.

The Attitude Heading Reference System (AHRS) provides aircraft roll, pitch and heading to aircraft flight instruments, automatic flight control systems and to on-board computers for navigation computations. The AHRS output data are combined with doppler radar and/or air data to provide dead reckoning navigation, but do not provide as accurate or self-contained navigation as that of an inertial navigation system (INS). However, the AHRS has been historically 20 percent of the cost of an INS. The AHRS serves as the primary reference of aircraft roll, pitch and heading in non-INS-equipped aircraft, such as helicopters, and as a back-up reference in aircraft equipped with an INS. The AHRS senses vertically to a lesser degree ($\pm$ 0.5) than does the INS. However, magnetic north is sensed by the aircraft magnetic azimuth detector and the AHRS gyro is slaved to that sensor. The resultant system accuracy for heading is approximately 1.0 degree.

6.2.7.2 Current Capability and Identified Deficiencies

Current operational capability is represented by systems in service, such as the A/A24G-39 and the AN/ASN-116 which utilize gimbaled platforms. The A/A24G-39 is a first order AHRS which does not utilize external measurements of velocity. The AN/ASN-116 is a second order AHRS which utilizes external measurements of velocity, such as those from doppler radar or air data, to obtain improved vertical accuracy.

The equipments in service are providing Navy aircraft with a primary or back-up source of roll, pitch and heading information. However, a number of deficiencies can be identified. Reliability and maintainability are lower than desired. The pitch and roll accuracies of AHRS equipment, especially those of first order, are not adequate under all maneuvering conditions. The equipments in service have withstood all severe environments encountered in the areas of vibration and corrosion. Some equipments designed for the fixed wing aircraft environment have experienced degraded performance when utilized in rotary wing aircraft. Periodic calibration of equipments in service, in order to compensate for errors in the Magnetic Azimuth Detector, is typically a time-consuming, inconvenient procedure. Whenever an aircraft engine is changed, for instance, there exists a requirement to compensate the heading system to account for the variation of the effect of the different engine. The equipments in service either provide no digital outputs or are not compatible with standard digital interfaces such as MIL-STD-1553 multiplex systems. In some cases, analog outputs are not easily interfaced with other aircraft systems due to inadequate synchro power or a lack of provision for separate, external excitation of each synchro.

6.2.7.3 Equipment Development and Modernization

The principal new development to modernize current in-service equipment is the strapdown AHRS. The strapdown AHRS utilizes a digital computer and body-mounted gyros and accelerometers instead of a gimballed platform. Designs have been under development and commercial versions are entering the production stage. The strapdown AHRS is expected to replace the A/A24G-39

equipment, which was originally planned for use in the SH-60B aircraft. Once the replacement program is approved, approximately two years will be required to develop and demonstrate the strapdown AHRS for use in the SH-60B aircraft, prior to production.

The strapdown AHRS in the SH-60B is expected to be a second order system with improved reliability and maintainability. It is expected to be qualified for use in rotary wing aircraft. The strapdown AHRS may permit rapid calibration to compensate for errors in the Magnetic Azimuth Detector. It will provide analog outputs with sufficient output power and separate, external excitation of each synchro. The replacement strapdown AHRS for the SH-60B may not be compatible with MIL-STD-1553 multiplex systems without modification, because such compatibility is not required by the SH-60B avionics.

6.2.7.4 Summary of Requirements

Short Term (0 to 5 years) -

* Evaluate the strapdown AHRS developed for the LAMPS MK III program on a technical and life cycle cost basis for possible use in the Conversion In Lieu Of Procurement (CILOP) of other Navy aircraft.

* Develop a strapdown AHRS with a MIL-STD-1553 compatible digital data interface.

* Develop an AHRS that senses the earth's electrostatic field and derives verticality.

* Develop a strapdown AHRS which can be upgraded to full INS capability by changing software and incorporating improved gyros.

* Perform life cycle cost trade-off studies to identify design changes with potential for cost savings for a strapdown AHRS.

* Incorporate identified design changes for reduced life cycle cost.

* Develop a software routine to utilize the Magnetic Azimuth Detector output and add it to mag variation to obtain true heading and utilize this parameter in a comparative circuit for dual inertial systems.

* Develop a pre-calibrated, pre-indexed Magnetic Azimuth Detector.

* Develop strapdown AHRS which have automatic compass calibrating features for single and double cycle errors.

Mid Term (5 to 10 years) -

* Evaluate use of a fully capable INS in place of a strapdown AHRS on each model of Navy aircraft with an AHRS. For aircraft with

AHRS as a backup to an INS, evaluate use of dual INS in place of a single INS with AHRS backup.

* Incorporate strapdown AHRS in CILOP of Navy aircraft which do not use a dual INS configuration.

Long Term (10 years plus) -

* Replace current and strapdown AHRS with a fully capable INS or upgrade strapdown AHRS to a fully capable INS in appropriate aircraft. Retain strapdown AHRS in remaining aircraft or complete CILOP to incorporate strapdown AHRS.

* Major development of an advanced AHRS beyond the near and mid-term AHRS is not required. Requirements can be met by either the near and mid-term AHRS or by an INS.

6.2.7.5 Development Priorities

Strapdown AHRS with a MIL-STD-1553 compatible digital data interface which can be upgraded to full INS capability.

Life cycle cost study to identify cost advantages, if any, of dual INS versus INS/AHRS.

Improving accuracy of AHRS gyros while minimizing increase in gyro cost by employing new technology, such as molded plastic gyros, so that strapdown AHRS can be upgraded to full INS capability.

6.2.8 CORRELATION VELOCITY SENSOR (CVS)

6.2.8.1 Background

Currently, the requirement exists for Navy aircraft to possess a self-contained navigation capability. Therefore, Inertial Navigation Systems (INS) are installed on most Navy aircraft to provide an independent navigation capability. INS systems utilize gyroscopes in conjunction with accelerometers to provide navigation information. However, in order to obtain vehicle velocity and position from the INS, it is necessary to mathematically integrate the accelerometer data (single and double integrations for velocity and position respectively); this technique introduces cumulative integration errors which are a direct function of time. Thus, left "undamped", INS velocity and position errors will grow with time. Therefore, it is desirable to bound INS errors by using alternate, self-contained means of measuring aircraft ground velocity to update and damp INS-derived velocity and position. Also, in most rotary wing aircraft, only Attitude Heading Reference Systems (AHRS) are installed. As the name implies, AHRS only provide direction and attitude information to the pilot. In these aircraft, continuous ground velocity measurements are a necessity to provide full navigational capability to the pilot.

6.2.8.2 Current Capability and Identified Deficiencies

To date, Doppler Velocity Sensors (DVS) such as, AN/APN-153, 141, 190 and others, are used extensively in military aircraft to update and damp

the INS-derived ground velocity and position. However, due to drawbacks inherent to the DVS technique, DVS measured velocities are often unreliable and unused. The major DVS problem areas are as follows:

* Over-the-water bias error, typically in the order of two to six percent of vehicle velocity.

* Loss of return signal over smooth water (sea state 1 or below).

* Relatively large allotment of vehicle surface area (0.2 to 0.4 m^2) for high gain antennas.

Indeed, mission data statistics collected from the P-3C aircraft showed that DVS is effectively used only 50 percent of the time.

6.2.8.3 Equipment Development and Modernization

The solution now being undertaken by NAVAIR is the development of the Correlation Velocity Sensor (CVS). The CVS approach utilizes statistical correlation of terrain microwave backscattering signals among several identical receiving antennas to calculate aircraft ground velocity. The CVS technique is inherently superior to DVS in terms of over-the-water performance, simplicity, and relatively small antenna requirements. Furthermore, the results of the planned development will be applicable to all Naval rotary wing, fixed wing, and VSTOL (Vertical/Short Take Off and Landing) aircraft.

Preliminary brassboard models of CVS were evaluated in laboratory and flight tests. Results of flight tests demonstrate proof-of-concept as well as over-the-water superiority of CVS over DVS. Information derived from flight tests are currently being utilized for brassboard model diagnostics and improvement. Follow-on exploratory development will continue on brassboard models showing the best potential of success. Transition into Advanced Development Models (ADMs) is planned for FY 83, followed by initial operational capability by FY 87.

6.2.8.4 Summary of Requirements

Short Term (0 to 5 years) -

* Develop full functional brassboard CVS model(s).

* Transition into ADM and develop ADM specifications.

* Fabricate ADM hardware.

* Development, test and evaluation of ADM hardware.

Mid Term (5 to 10 years) -

* Development of Engineering Development Model (EDM) specifications.

* Fabricate EDM hardware; conduct flight tests and evaluations.

* Installation and integration with candidate aircraft.

Long Term (10 years plus) -

* Replace all DVS with CVS in military aircraft.

* Install CVS in all advanced Naval aircraft.

6.2.8.5 Development Priorities

* Develop correlation velocity sensors which are superior to existing CVS in terms of life-cycle cost, over-the-water performance, and smaller antenna requirements.

* Replace DVS with CVS and install CVS in advanced Naval aircraft.

6.2.8.6 Ongoing Program

Correlation Velocity Sensor (CVS)

MILESTONES

FY 82
Full functional brassboard model flight tests

FY 83
Transition to ADM

FY 85
ADM DT&E

6.2.9 JOINT TACTICAL INFORMATION DISTRIBUTION SYSTEM (JTIDS) - TACTICAL AIRBORNE NAVIGATION (TACAN)

6.2.9.1 Background

There is a continuing requirement for an accurate short range line-of-sight navigation system for all Navy aircraft. TACAN is the Navy's primary airborne short range navigation system. TACAN navigation information provided to Navy users is comprised of range, bearing and identity tone supplied by a surface beacon. Communication of the navigation information is via a radio frequency (RF) link in the frequency band of 962 MHz to 1213 MHz. The Navy's airborne TACAN system incorporates an air-air ranging feature for tactical applications. The TACAN system was initially developed by the Navy; however, it has subsequently become a world-wide standard with heavy concentrations of surface beacons in the Continental United States and Europe. The system operates on a low duty cycle - approximately five percent; i.e., five percent of the available transmission time is occupied. Present state-of-the-art positional accuracy measurable by an airborne user is $\pm$ 0.5 degrees and $\pm$ 0.05 nautical miles to a ground beacon.

6.2.9.2 Current Capability and Identified Deficiencies

Present military airborne TACAN systems are comprised of two types: older units such as the AN/ARN-52(V) with analog processing, and units like the AN/ARN-84(V) and AN/ARN-118(V) that utilize digital processing logic. These systems feature accuracies of + 1.0 degree for bearing and + 0.1 nautical mile for ranging and provide Morse coded aural tone for identifying each ground beacon. All weigh approximately 50 lbs and have similar physical dimensions. One of these units is required in all Navy and Air Force tactical aircraft. This requirement will continue into the foreseeable future. The AN/ARN-84 and the AN/ARN-118(V) are satisfactory in performance and reliable. However, they could be completely replaced when JTIDS is implemented.

6.2.9.3 Equipment Development and Modernization

Since the TACAN system is a low duty cycle occupant of the frequency band (962-1213 MHz) and has a high degree of immunity to atmospheric effects, RF designers have proposed new concepts in secure data communications that would co-occupy the TACAN frequency band. The principal system targeted for ultimate frequency co-occupancy is JTIDS. JTIDS is presently under tri-service development by the Navy, Air Force and Army. This JTIDS system combines the airborne TACAN function with several data communication functions, all under the control of a central computer.

The JTIDS terminals currently being developed may operate in a JTIDS/TACAN mode, a TACAN only mode, and a JTIDS only mode. The TACAN and JTIDS relative navigation parameters are computed by separate Kalman filter algorithms. The Kalman filter for the TACAN mode uses the distance and bearing information transmitted by the TACAN ground station as inputs, and oututs an accurate range and bearing estimate. The Kalman filter algorithm for the JTIDS mode uses time of arrival of position messages, together with special round trip timing (RTT) messages and aircraft navigation system inputs to determine both relative and geodetic position.

6.2.9.4 Summary of Requirements

Short Term (0 to 5 years) -

* Examine the potential of removing TACAN sets in those aircraft which will be equipped with JTIDS terminals.

* Develop software algorithms for combining JTIDS relative navigation information with the JTIDS TACAN information.

Mid Term (5 to 10 years) -

* Study the possibility of removing the TACAN beacon transponder from naval vessels to eliminate interference with ships JTIDS terminals. Replace the TACAN waveform with a JTIDS waveform being transmitted through the TACAN mechanical AM modulator antenna. TACAN-type range and bearing accuracies could be obtained with JTIDS pulses having TACAN AM modulation.

Long Term (10 years plus) -

* Implement TACAN/JTIDS beacon systems

6.2.9.5 Development Priorities

The development of software to include TACAN range and bearing estimates in the JTIDS relative navigation processing should receive attention. Shipboard applications which require a TACAN beacon capability will present a compatibility problem which must be resolved prior to JTIDS introduction to such operational units. Alternatives such as new antenna designs and amplitude modulation of JTIDS pulses should be evaluated to determine a cost effective solution.

6.2.9.6 Ongoing Programs

There is a program for developing an antenna for shipboard use to provide isolation between TACAN, GPS, and JTIDS terminals.

There are several programs in the analysis area which are currently funded.

* JTIDS/UHF Performance Analysis - The objective of the performance analysis is to evaluate JTIDS and UHF communications systems in task group scenarios.

* JTIDS Net Management Studies - The JTIDS net management studies are being performed to determine how JTIDS may best be implemented in the Fleet.

* Navy Command and Control Requirments Data Base - The requirements data base is being developed and maintained to consolidate information and to facilitate validation of command and control requirements for OPNAV.

6.3 COMPUTERS/DATA PROCESSING

The field of militarized computers/software continues to change very dynamically as new concepts and technologies foster new capabilities and almost simultaneously create a demand for still more capabilities. The key to controlling life cycle support costs for today's complex and highly capable software intensive weapons systems lies in standardization. The Navy has chosen to standardize at the support software level, i.e., the compilers, assemblers, simulators and system tape generators, and at the programming language level, i.e., CMS-2 and SPL-1. These are the software standards which are common to hardware standardization development efforts of the AN/AYK-14(V), the AN/UYK-44(V) and, to an extent, the AN/AYK-( ), the future or next generation airborne standard computer. The development of ADA will gradually produce a shift away from today's standard higher order languages CMS-2 and SPL-1, particularly for the AN/AYK-( ). Proper utilization of the technological advances which the Very High Speed Integrated Circuits (VHSIC) program is expected to produce will permit the Navy to develop a more powerful, smaller and more reliable future generation standard airborne computer.

As the Navy completes the development and enters the production phase for the AN/AYK-14(V) Standard Airborne Computer, it begins the development of the AN/UYK-44(V) Militarized Reconfigurable Computer and must almost simultaneously, in order to meet the challenge of the future, begin the planning for a future generation standard airborne computer. Figure 6-6 indicates the Major Milestones for each of these programs. The Navy remains firmly committed to standardization as the key to controlling life cycle support costs. Identified and projected requirements for the AN/AYK-14(V), the AN/UYK-44(V) and the AN/AYK-( ) are shown in Figure 6-7.

The following sections present a summary of on-going computer standardization efforts as well as identify future requirements that must be satisfied through aggressive development efforts. These planning data provide the foundation for new or updated acquisition plans. As new Fleet needs are identified, new task elements will be defined and incorporated in subsequent issues of the NAMP.

6.3.1 STANDARD AIRBORNE COMPUTER AN/AYK-14(V)

6.3.1.1 Background

Since the early 1960s, many computers have been developed to fulfill the computational requirements of various airborne platforms/systems. This relatively large number of functionally similar, but logistically unique, computers created a major logistics support problem for the Navy. By its very nature, computer hardware is highly complex and enters the Fleet as near-state-of-the-art technology. More significantly, the support of the computer software has reached a level that surpasses support of the hardware. Because of the enormous support required by both computer hardware and software, the Navy is currently pursuing a course which will reduce the life cycle costs for computer controlled avionics systems. To this end, the Navy has addressed the problem of proliferation of computer types and software languages through the development of the Standard Airborne Computer AN/AYK-14(V) which utilizes Common Support Software AN/UYK-20(V).

6.3.1.2 Current Capability and Identified Deficiencies

The AN/AYK-14(V) development is NAVAIR's first endeavor to establish a Government Furnished Equipment standard airborne computer. The AN/AYK-14(V) provides an improved performance capability in a central computer which enhances the capability of airborne weapons systems. More significantly, the AN/AYK-14(V) provides the Fleet with a standard computer which is logistically supportable.

The Standard Airborne Computer AN/AYK-14(V) design was modularized in order that the computational, Input/Output (I/O), and memory requirements of many avionic systems through the 1990s could be fulfilled by reconfiguration of the AN/AYK-14(V) module set. The AN/AYK-14(V) has both volatile semiconductor and non-volatile core memory addressing capability of 512K (K=1024) words. A variety of I/O interface channels are available including Navy Tactical Data System (NTDS), MIL-STD-1553A, PROTEUS and RS-232. Five unique chassis types are available to house the AN/AYK-14(V) modules, or the modules may be embedded directly in a weapons system. The modular design will permit

MAJOR MILESTONES FOR AYK-14, UYK-44 AND AYK-( )

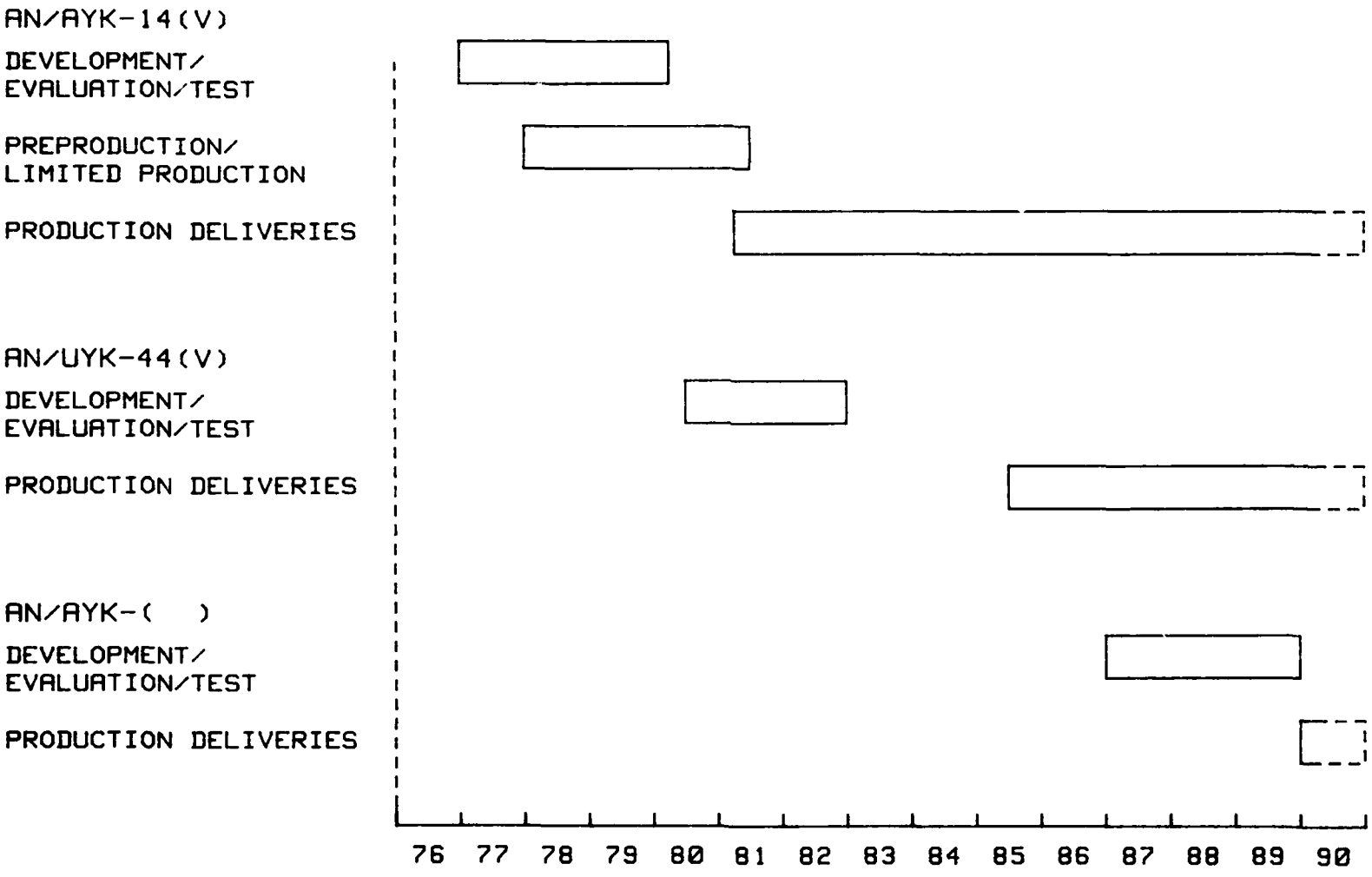

FIGURE 6-6

PROJECTED CUMULATIVE COMPUTER SYSTEMS

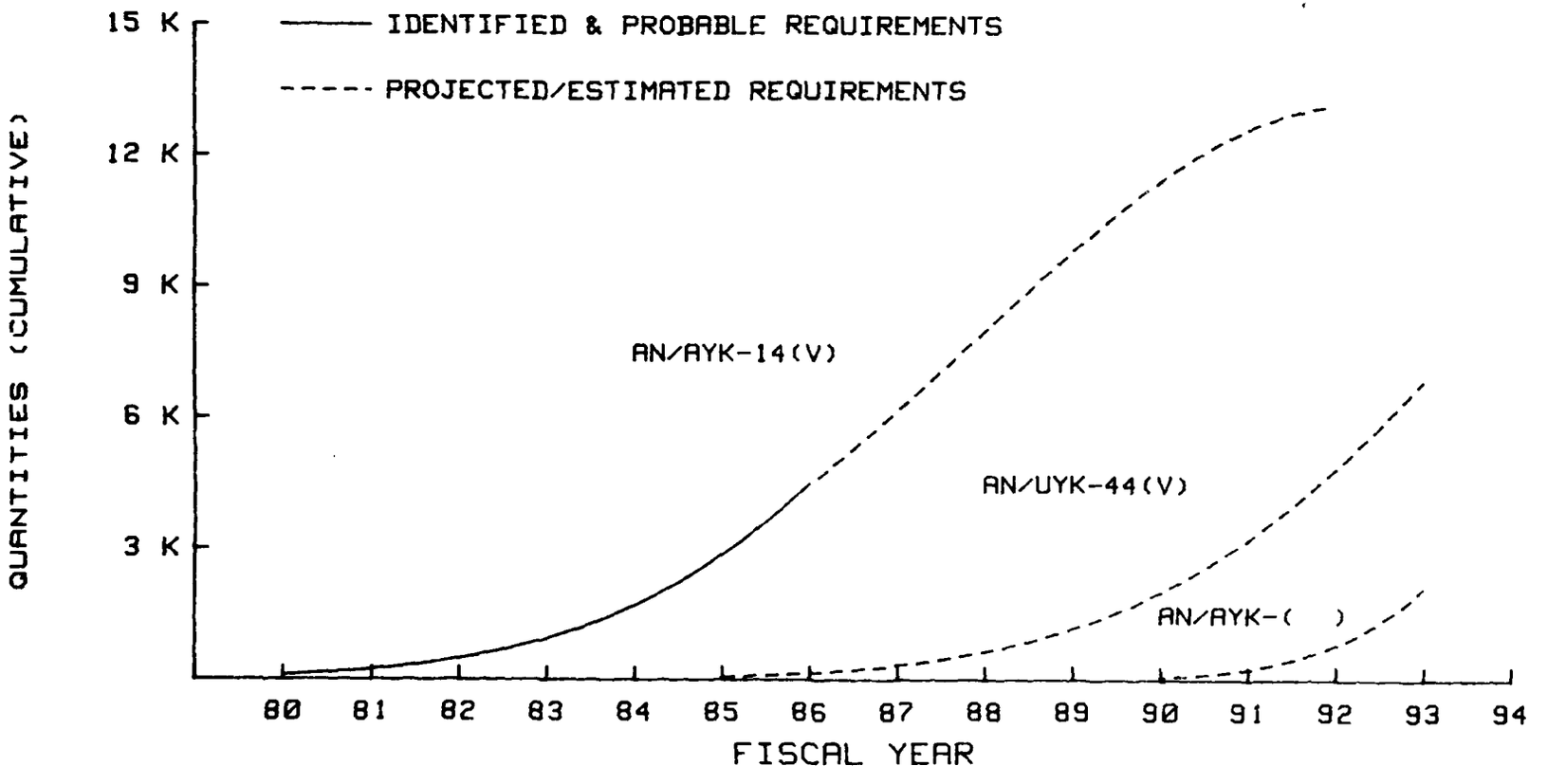

FIGURE 6-7

use of the AN/AYK-14(V) in a wide variety of airborne weapons systems through 1990. Commonality in the subassembly and spare parts inventory permits logistics savings by all platforms using the AN/AYK-14(V).

The AN/AYK-14(V) emulates the Standard Shipboard Computer AN/UYK-20(V) and utilizes the instruction set and the Machine Transferable Support Software package (MTASS-20) already established for the AN/UYK-20(V). Operational software programs for the AN/AYK-14(V) may be written in the Navy's standard high order language (HOL), CMS-2. This GFE support software/ instruction set standardization provides the Navy with improved capability to support and maintain the tactical operational software and to significantly reduce costs over the life cycle of the sytems. Additional savings are realized by utilizing a single set of diagnostic software for the AN/AYK-14(V) family of "standard" modules.

A single site Software Support Activity (SSA) has been established to support AN/AYK-14(V) common software; i.e. diagnostics, microcode, and bootstrap loader. Operational/tactical software programs will be maintained by the individual weapons systems support activities.

The modular design and functional subsystem architecture of the AN/AYK-14(V) allows considerable flexibility in terms of upgrading the computer to overcome identified deficiencies. The AN/AYK-14(V) does not currently have the capability to provide an input/output interface to MIL-STD-1553B compatible devices. In addition, the operational software requirements of some weapons sytems have grown to the point where additional memory capacity will soon be required. NAVAIR has developed plans and budget requirements to correct both of the above deficiencies.

6.3.1.3 Equipment Development and Modernization

Since the completion of the development phase of the AN/AYK-14(V), new requirements have become evident for this standard airborne computer. The introduction of the requirement for use of MIL-STD-1553B (in lieu of MIL-STD-1533A) has created the need for the development of this interface module. Additional I/O interfaces and redefinition of existing I/O interfaces, i.e., NTDS-ANEW additional features and a PROTEUS interface change, have resulted in the development of new hardware. Technological advances in the density of core memories have resulted in the capability to double the capacity of the AN/AYK-14(V) core memory in the same physical volume. The introduction of these modules will increase the AN/AYK-14(V) capability to meet growing user needs.

The use of the standard executive, SDEX/M should be encouraged (not mandated). Since it is a new, untried program, user feed-back should be carefully monitored as a basis for improvements. To avoid duplication of development efforts of other real-time software, a user exchange could be established so that operational modules developed by one program would be available to others.

6.3.1.4 Summary of Requirements

Short Term (0 to 5 years) - The Navy has identified firm requirements for over 4,000 AN/AYK-14(V)s through the FY 86. Known requirements by

fiscal year are shown in the table below. It is probable that other applications for the AN/AYK-14(V) will develop in this time frame and it is estimated that an additional 2,000 to 4,000 production units will be required to satisfy these applications. During this period of time, the AN/AYK-14(V) family of modules will be expanded to satisfy the requirements of new applications. Potential new modules include an Enhanced Input Output Processor (EIOP), Direct Memory Access (DMA) interface module, 28 Vdc Power Supply, analog/digital and digital/analog (A/D and D/A) conversion interfaces, and other I/O types determined by specific user needs. Near the end of this time period, new applications will tend to migrate toward the next generation standard computer; however, production of AN/AYK-14(V)s to fulfill continuing requirements for existing weapons systems will continue through 1990.

FY 80	FY 81	FY 82	FY 83	FY 84	FY 85	FY 86
130	160	270	420	700	1,055	1,360

Mid Term (5 to 10 years) - AN/AYK-14(V) production will continue during this timeframe in order to meet the requirements for users who have designed their systems around the AN/AYK-14(V) in its development and early production phases. The end of this period will see a gradual decline in the rate of production as future "standard" computer developments phase in. The total number of AN/AYK-14(V)s produced during this timeframe is estimated to be 2,000 to 3,000 units.

Technology is expected to continue to advance at an increasing rate and, as is currently the case, will continue to be driven by commercial industry. Proper utilization of technology improvements will become a high priority in the computational arena. The Navy has, and will continue to push the system requirements higher and higher to meet its performance and operational readiness goals. Proper planning and supporting guidelines will enhance the Navy's abilities to attain these goals in the technical, management, and support areas. These factors will drive the AN/AYK-14(V) toward obsolescence and see the advent of a new AN/AYK-( ) for use in new weapons system developments.

Long Term (10 years plus) - The AN/AYK-14(V) effort in this time frame will primarily be the support of the equipment and the software in the Fleet use. System designers will be selecting the AN/AYK-( ) family for new system developments.

6.3.1.5 Development Priorities

MIL-STD-1553B usage in any new avionics system utilizing a bus system is a Navy requirement. Since the AN/AYK-14(V) currently has an "A" version of the MIL-STD-1553 interface, the "B" version of this standard interface is a high priority development requirement. Double density core memory modules have been developed that will operate in the AN/AYK-14(V). A testing/verification effort is required to qualify this memory module as a part of the AN/AYK-14(V) family. Many users, including the F/A-18 and P-3C have indicated a need for additional memory capacity.

Development of the Enhanced Input Output Processor (EIOP) and Direct Memory Access (DMA) interface modules will be very advantageous to a number of current and potential AN/AYK-14(V) users. These developments will be studied very closely so as to achieve the maximum benefit from the technology available.

6.3.2 STANDARD AIRBORNE COMPUTER AN/AYK-( )

6.3.2.1 Background

A requirement is developing for a next generation standard airborne computer that will take advantage of advances in technology and design concepts. A program to accomplish this must be initiated in the near timeframe. Driving factors for this effort will include increased capabilities available from emerging technologies, needs for smaller building blocks in order to fit into smaller overall form factors, and requirements for less power consumption and higher reliabilities.

6.3.2.2 Current Capabilities and Identified Deficiencies

The total requirements and design concepts for this effort must be defined. This will involve a major coordination effort in identifying potential users willing to invest in this concept, and combining the requirements of all identified users to define the overall development effort.

Provision should be made for multiprocessing (as distinct from distributed processing). That is, it should be possible to vary the number of processors executing from a single memory system, with a corresponding increase in performance.

Areas of consideration in such a program should include:

* Fault tolerance,
* Distributed processing compatibility,
* Throughput,
* Higher Order Language compatibility,
* Technology transparency,
* Subsystem independence, and
* Module Independence.

6.3.2.3 Equipment Development and Modernization

The Very High Speed Integrated Circuit (VHSIC) program will have a major effect on an AN/AYK-( ) development. This six year program, started in 1979, was initiated to provide a major jump in DOD's embedded computer capabilities by as much as two orders of magnitude in throughput, together with similar reductions in size, weight, and power. Emphasis in the program is

placed on integrated circuits (ICs) for special purpose embedded computers for signal processing applications; however, general purpose computers are not excluded. Indeed, many VHSIC proposals for Phase I include the development of a general purpose data processor brassboard subsystem. The success of the VHSIC development will be a primary factor in determining the final configuration of the AN/AYK-( ) hardware.

6.3.2.4 Summary of Requirements

Short Term (0 to 5 years) - This timeframe will be devoted to defining the requirements applicable to the AN/AYK-( ). Concepts must be developed and potential users must be identified to fund the effort. All the data must be combined into a solicitation package and resources must be identified within the Navy to staff the management of the program and otherwise support the development effort.

Mid Term (5 to 10 Years) - The full-scale development of the AN/AYK-( ) will be a priority task. In new technology utilizations, such as would be applicable to the AN/AYK-( ), there are several features of prime importance. Some of these have been introduced and accepted while others are in their infancy. A new computer development, the AN/AYK-( ), must utilize the following features in order to be a state-of-the-art machine:

* Fault Tolerance - As computers become faster, smaller, and more powerful (in terms of throughput, I/O speeds, etc.), they lend themselves to utilization of redundant features to provide fault tolerance, which is an absolute requirement for mission critical functions. With reductions in size and weight allowed by advancing technology, computational systems can attain near complete redundancy such that the computer system will reconfigure itself when self test features isolate a faulty component/subassembly. It will be a requirement to have, at the very worst case, a graceful degradation of the computational capability of the system when a failure occurs, and preferably only relatively small interruptions or slowdowns to the system.

* Higher Order Language Compatibility - Navy software in the future will be written in a standard, higher order language (ADA). Provisions must be made in the AYK-( ) instruction set to provide easy, efficient compilation (or perhaps even direct execution) of ADA constructs.

* Technology Transparent Functional Partitioning - An important consideration in the development of any new computer system is the degree to which the functional partitioning produces technology transparency. Careful design of the internal bus structure is key to producing a computer which will permit technological update. It is the computer bus (or buses) which allows all data to be transferred between elements of a system. The bus determines the word size (i.e., 8 bit, 16 bit, etc.), the maximum data transfer rate, and the protocol. Lack of bus structure planning results in a computer with functional capabilities that are quickly over loaded, and quickly disappearing growth potential.

* Memory Independence - There should be a central memory for the system connected to the main buses. The memory subsystem should have its own BIT for power up initialization and checkout, along with continuing diagnostic capability. One of the features of the memory would be a "pool" which would contain packets of information defining which processor (or I/O) was working on a particular area in memory. This would allow coordinated inter-task communication.

* I/O Independence - For external communication, completely independent I/O modules should be added to the system. Each of these modules would have the above described usual dual bus interface along with on-board memory to buffer relatively large I/O transfers. A BIT function should be available for each of the I/O modules, and module testing would be performed whenever the module was not in use.

* Self Contained BIT - As has been previously alluded to, each functional module (such as a CPU with its local bus, or an I/O, or the memory) would have its own BIT. These BITs would individually check each board and the arbitrators would have the function of checking the BITs to ensure proper operation. This self-contained BIT at the board level would reduce dependence on complex diagnostic programs to isolate faults to the module level. On-board BIT would also facilitate second sourcing to a functional specification at the module level.

Long Term (10 years plus) - The long term requirements for the AN/AYK-( ) will be the introduction of the new computer into the Fleet. The increased requirements for system performances will mandate new computers, using the VHSIC type technology. The technology will also avail itself to using computer technology in almost every avionic subsystem, a trend that is emerging even today. Performance requirements will not allow the stagnation of technology improvements, and in this long term time frame, planning will begin on the next generation avionic computer(s).

6.3.2.5 Development Priorities

The VHSIC development program has the highest priority in the realm of a future AN/AYK-( ) program. Although there is no direct tie between VHSIC and a possible new standard airborne computer, the Navy does intend that a VHSIC brassboard general purpose data processor be demonstrated.

The patterns of standardization evident in the AN/AYK-14(V) and the AN/UYK-44(V) must be carried on in future generations of computers such as the AN/AYK-( ) in order to minimize design, support, and documentation costs in the areas of both hardware and software. New technologies and new packaging concepts to meet future requirements will result in additional families of spare subassemblies/spare parts and these evolutions are expected. However, the effect on the maintenance costs can be minimized by developing "standard families" of modules that are used across many platforms. A huge saving is resulting in the use of the established AN/UYK-20(V) instruction set and MTASS-20 support software across the AN/UYK-20(V), AN/AYK-14(V), and the

AN/UYK-44(V) programs. Only minor modifications to the support software are required in lieu of costly development of a completely new support software package.

The future generation of a standard airborne computer, AN/AYK-( ) will again have a common family of modules tailored to the electronics and packaging technologies of the development period. The AN/AYK-( ), due to advances in computer architecture, will probably find it advantageous to implement a modern, HOL oriented architecture. Programming may be performed in CMS-2 , SPL-1, or the upcoming HOL "ADA."

6.3.3 MILITARIZED RECONFIGURABLE COMPUTER AN/UYK-44(V)

6.3.3.1 Background

Through the 1970s, many of the Navy shipboard processing needs were satisfied by the Standard Shipboard Computer AN/UYK-20(V). In the late 1970s, limitations of the AN/UYK-20(V) became evident and the AN/UYK-44(V) program was evolved. The AN/UYK-44(V) development promises increased throughput, more memory, and I/O capability than its predecessor. The contract for development of the AN/UYK-44(V) was awarded in September 1980.

6.3.3.2 Current Capability and Identified Deficiencies

The AN/UYK-44(V), in a concept similar to the AN/AYK-14(V), is being developed as a modular, reconfigurable computer/processor under the auspices of NAVSEA using, primarily, ISEM-2 (Format B) size modules as building blocks. Although primarily for shipboard users, the modules will be qualified for use in the airborne environment to permit use by system designers in both areas. Like the AN/AYK-14(V), the modules can be independently embedded in a users system to met his unique requirements. The AN/UYK-44(V) will also use CMS-2 HOL and the MTASS-M support software package common to the AN/UYK-20(V) and the AN/AYK-14(V).

6.3.3.3 Equipment Development and Modernization

As with the AN/AYK-14(V), the AN/UYK-44(V) will evolve to meet the changing requirements of the users. This will include the MIL-STD-1553B, fiber optics, and other I/O interfaces, in addition to more memory and higher speed requirements. As the AN/UYK-44(V) design becomes firm, additional requirements and changes to existing requirements will drive efforts not necessarily foreseen at this time. These development changes are common for a highly complex, state-of-the-art, militarized piece of equipment.

6.3.3.4 Summary of Requirements

Short Term (0 to 5 years) - The AN/UYK-44(V) will transition from the development phase to the production phase within the next five years. Experience with the AN/AYK-14(V) indicates that related developments on the AN/UYK-44(V) will continue past the five-year mark. This evolution, as new users begin using this system, is essential to the viability of the AN/UYK-44(V) as a standard computer system.

* Areas the Navy will have to closely monitor during this development period include the following:

  * Qualification of all modules to both avionics and shipboard requirements.

  * Implementation of the AN/UYK-20(V) instruction set with enhancements so that changes are minimized and any changes made are fully documented and promulgated.

  * Definition of interface characteristics of the modules/module groups such that a system designer can embed the modules in his system.

Mid Term (5 to 10 years) -

* In 5 to 10 years, the AN/UYK-44(V) will enter a major production phase reflecting the production of avionics systems designed during the late development/early production phase of the AN/UYK-44(V) program. Also, near the beginning of this timeframe, users will find bugs in the system, putting a heavy burden on personnel involved with both hardware and software configuration control of the AN/UYK-44(V) design.

* It is expected that several airborne systems, especially those to be designed using embedded processor modules, will utilize the AN/UYK-44(V) modules in this timeframe.

Long Term (10 years plus) -

* The AN/UYK-44(V)/module set will be a major consideration with system designers, due to its maturity and its smaller size than the AN/AYK-14(V). At this point in time, the AN/AYK-14(V) technology will be approaching the point of obsolescence, steering system designers away from the AN/AYK-14(V). Consequently, the AN/UYK-44(V)/modules will become the "current" designer's choice. For systems to be developed with "state-of-the-art" technology, the choice will be the AN/AYK-( ).

6.3.3.5 Development Priorities

* define module interface requirements.

* module qualification.

* document AN/UYK-20 instruction set enhancements.

6.3.4 ADA

6.3.4.1 Background

Higher order software languages did not have their beginnings until some 15 years after the first computers were developed. In the 1940s, industry and government saw a need for moving away from binary programming of the

computers, that is, to have the capability of using some sort of mnemonics or assembly instructions to represent or produce the machine code which the computer could use. This was basically the origin of assembly languages, and the resulting increase in the amount of code a programmer could produce. These were soon followed by Higher Order Languages such as FORTRAN and COBOL, developed by the scientific and government communities, respectively. In the primitive field of computational use during the 1940s and 50s, these first Higher Order languages received large acceptance and became standards. In the 1960s, however, and especially in the 1970s, more and more languages were thrown into the computer arena as the programming community saw the inherent limitations to languages such as COBOL, FORTRAN, and BASIC. Specifically, these languages did not necessarily promote programming which was easy to maintain, nor was this software easily testable or understandable. This situation was aggravated as computer hardware costs steadily dropped, and computer system parts (such as memory, discs, and processing speed) increased on a seemingly exponential curve. The major difficulty with software in the 1970s was that there were such a large number of software languages available, a standard could not be chosen, even though it was clear that the proliferation of languages could not continue. Some attempt had to be made to lower software costs to bring them back into line with hardware costs.

To this end, the Department of Defense, in the latter half of the 1970s, coordinated with the user community to develop a new standard software language. The result of this effort was ADA. Over 20 languages were studied as candidates for change or upgrading for the development of the new ADA language. In the end, it was determined that no present language could be modified, and a new language would have to be developed to suit as many user needs as possible. ADA was a very risky undertaking because of the new development effort, and user acceptance was at stake. The structured language PASCAL was used as a base for much of ADA. It was expanded to include such attributes as concurrent processing, interrupt processing, and exception handling capabilities.

As of the summer of 1980, the entire ADA package had been frozen and defined, and a contract was underway to develop the first ADA compiler.

6.3.4.2 Current Capability and Identified Deficiencies

The actual definition of the ADA language is now complete, and the language is currently awaiting compilers. ADA should have approval from a standardization committee such as the Institute of Electrical and Electronic Engineers (IEEE) such that subsets and supersets of the language are not promulgated, and destroy the standardization attempt.

There are perhaps no known deficiencies with the ADA language, as it has just been developed, and no compilers have yet been implemented. Enthusiasm for the language is not at a high level, perhaps due to the fact that when a new language is developed, it generally takes several years before sufficient experience has been accumulated to squelch user concern about compiler reliability.

6.3.4.3 Equipment Development and Modernization

Currently, the Army is the only one of the three services which has awarded a contract for the development of an ADA compiler. A compiler for the Digital Equipment Corporation VAX 11/780 32-bit computer is currently being developed. Contracts for ADA compilers will shortly be let by the Air Force. Additional compilers should be adapted/developed as quickly as possible by the Navy, such that ADA can go into use in the very near term.

6.3.4.4 Summary of Requirements

Short Term (0 to 5 years) -

* The first five years or so of a programming language will determine whether it has the capability of becoming an accepted standard. Merely naming a language as a standard in today's software world does not make it so. For any programming language to become widely used, it must meet at least the following requirements:

  * Functionality - The language must have a wide range of constructs capable of handling programs from a wide area of applications (such as real-time, data base work, interrupt environment, and I/O bound systems).

  * Performance - The language should make efficient use of the computer systems resources (such as memory, disc, and tape subsystems) and should be capable of compiling programs relatively quickly.

  * Availability - For the language to be used at all, compilers for it must be available on as many computers as possible; mainframes, minicomputers, and microprocessors.

  * Reliability - The language should provide consistent results in accordance with its specifications. There should be no hidden characteristics that programmers can use or misuse.

  * Portability - Programs written in the language for one computer must be capable of being moved, or transported, to another computer with a minimum of change. In other words, there should be as few machine dependent functions or constraints on the language as possible. In the past, some of these constraints have been in areas of computational precision, interrupts, and perhaps especially, I/O ability.

  * Ease of Use - The language must be amenable to the programming situation which the programmer faces. The programmer should be able to easily mold the language constructs to fit his application.

  * Training - The language should not require extensive or costly training classes, and these classes and materials should be readily available.

  - * Operating Costs - The computer which hosts the compiler for the language should not be unduly burdened by the compiler itself. That is, the compiler must not require special system resources, and it should be sufficiently fast running such that the host can continue with other tasks which it must perform as quickly as possible.

  - * Acquisition Costs - The initial cost of the language (hence the compiler cost), should not place uncommon restrictions on the host machine, such as additional memory or discs. Also, installation time and true dollar cost must not be such sufficiently prominent figures that they hinder the acquisition cycle.

* The programmer or language developer, tasked with prioritizing the above list, would probably keep the list basically unchanged. The manager, however, would probably reorder it from the bottom up -- citing costs (initial buy, manpower, operations) as the major considerations. The disparity of views must be resolved in the near future.

Mid Term (5 to 10 years) -

* In the second half of the 1980s, possible refinements and additions to the ADA language will be required to fine tune it to user needs. These changes will come about due to the regular use which the language will see in various user applications.

Long Term (10 years plus) -

* ADA should receive wide acceptance and use by the 1990s, but users should not be surprised to find that many anomalies may exist in the language by that time. These problems can arise, for example, because programs which are not attempted with software today, may be commonly attempted with ADA, due to its higher level constructs. In essence, new questions will arise which are not known today, and these will manifest themselves as limitations on the present ADA language. At such a time, a new language must be developed to continue the lineage of standardization. This cycle may not have an end, since there is probably no such thing as the "ultimate" language.

* Additionally, as new hardware is developed, designers must lean toward integrated circuits (in particular, the microprocessors) which lend themselves to high level language use. This can be done, for example, by creating instruction sets which have such facilities as procedure calls, implementable by one instruction, and context switching, such that the machine state can be altered easily and quickly. As ADA becomes widespread it will be possible to design instruction set architectures which execute ADA programs directly, without the need for compilation.

6.3.4.5 Development Priorities

The Navy must endeavor to utilize the ADA languages as quickly as possible. Systems which are in use when ADA is available should not be asked to retrofit their software, but every effort should be made to utilize the new ADA language on systems which are under development or will be developed. ADA should also be considered a major candidate for use on those systems that will be upgraded.

6.3.5 EMBEDDED MICROCOMPUTERS

6.3.5.1 Background

Embedded digital computers have existed in Naval tactical systems since the 1960's. Recent advances in microprocessor technology have made numerous processing elements available for new processor development work. A microprocessor is a single-chip processing element (compatible support circuits may be required) capable of accessing memory and executing code or manipulating data. Memory is considered to be a separate entity from the microprocessor and contains instructions for the microprocessor to execute or data for the microprocessor to manipulate. Program memory is generally non-volatile Read Only Memory (ROM) while data memory is generally volatile Random Access Memory (RAM). A microcomputer is formed by adding RAM, ROM, and a limited amount of Input/Output (I/O), capability to a microprocessor. A microcomputer is a self contained, computational unit that is capable of performing a programmed task. A special class of microcomputers (analog I/O processors), have analog I/O capability incorporated into the chip. The efficient utilization of digital computers or recently developed microcomputers entails the development of both hardware and software standards to facilitate the implementation and maintenance of these units. The software standards to date include the use of the Higher Order Languages (HOL) CMS-2, SPL/I, and ADA. ADA is a planned Navy standard language that features strong type checking at the time of compilation to assure that data will be properly manipulated.

6.3.5.2 Current Capabilities and Identified Deficiencies

Avionics system architecture is moving away from the concept of one central computer to a distributed processing network. Typically, a distributed architecture is implemented by tying several independent computers to a common bus with each computer performing a single function, such as navigation, weapon or airframe control, or similar large scale efforts.

An extended version of this network is being used in newly developed avionics systems and is referred to as hierarchical architecture. Hierarchical computer structures consist of multiple processing levels with the system and mission processing at the top and subsystem processing at the bottom. The top level processors control the exchange of data over multiple sets of multiplex buses. The bottom level processors are most likely to be microcomputers or analog I/O processors used for digital-to-analog and analog-to-digital conversion, digital and analog signal and transform processing, filtering, thresholding, logical, and other operations.

The utilization of hierarchical structuring facilitates upgrading part or all of the avionic system and introduces standard interfaces into the subsystem. Once defined, the standard interface supports the application of the subsystem to other hierarchically-structured avionic systems.

Hierarchical avionic system architecture must support standardization and commonality to facilitate fault-tolerance and expandability. The hierarchical structure with redundant processors facilitates the redistribution of control and computation upon the occurrence of component failure or battle damage. Procurement and utilization costs of multiple microprocessor, microcomputer, and signal processors, combined with their small space and power requirements, permit the redundancy required to increase the reliability of avionics systems. Redundant microprocessor networks are within reasonable power and size limits as the multiplicity increases overall system reliability.

The greater availability of program storage space in smaller volumes allows the inclusion of Built-In Test (BIT) software in computers and processors throughout the hierarchy. The use of buses in avionics systems, over which many devices communicate, allows test and development equipment to be attached to the system to monitor a system in real time, rather than testing the devices individually after removal from the system. The test equipment can also query the individual processors to initiate BIT and, collect the resultant status information from each processor. The cost of maintaining all the languages now supporting Navy avionics systems is escalating each year. To reduce the expense of supporting new equipment, the Department of Defense has initiated the development of a standard HOL called ADA.

Although no compilers are presently available for ADA, its use in current and future Navy programs is being planned and discussed.

6.3.5.3 Equipment Development and Modernization

The development of one-chip microcomputers is presently being driven by commercial applications. Therefore, embedded one-chip microcomputers, which are generally 4 or 8 bit devices, will only gradually give way to 16 bit devices. Multi-chip microcomputer systems will generally be 16 bits, again with commercial rather than military applications driving the industry. The system computers on the top of the hierarchical ladder will tend to be 16 and 32 bit devices because they must possess the general purpose capabilities which are needed for these tasks.

As more avionic subsystems incorporate microcomputers and the software sophistication increases, the cost of software development, documentation, validation, and maintenance will become increasingly greater than development costs of the associated hardware. To reduce this software development cost, the use of in-circuit emulators will become more important. The utilization of in-circuit emulators allows processor register contents to be gathered in real-time situations and subsequently displayed for program verification and documentation. In-circuit emulators also permit single-stepping of instructions for software verification. During the development phase of hardware integration, in-circuit emulators can be used to perform hardware functional checks. Memory interfaces, I/O functions, and processor interaction can be verified by using in-circuit emulators.

6.3.5.4 Summary of Requirements

Short term (0 to 5 years) -

* Although there are some ongoing efforts, no current, effective standards exist in regard to the use of microprocessors and microcomputers. Current Navy specifications require the use of standard airborne computers to perform certain tasks that do not need the general purpose capabilities of relatively large standard computers. The small size, weight and power dissipation of microcomputers can be effectively utilized to solve many problems. Consequently, it is imperative to develop guidelines and/or standards in this area, so that the Navy can take advantage of current microprocessor technology.

* In the short term, the Navy will not be able to standardize on one microcomputer or microprocessor family because no chip or chip family exists that satisfies all of the needs for the next five years. The Very High Speed Integrated Circuit (VHSIC) program will not yield a family of chips for several years. The relatively low cost of current micro-devices and their programming capability will encourage the utilization of whatever best meets the requirements of the task. Several microprocessor houses are addressing the problems of software for present and future micros by developing ADA compilers for their chips.

Mid Term (5 to 10 years) -

* The need for "number crunching" exists at all levels of the hierarchy. The development of high speed single-chip arithmetic processors, input/output controllers, and analog I/O processors should be addressed by the Navy. The technology and techniques for producing these chips exist as evidenced by the availability of chips in commercial markets. The Navy should address the development of these same circuit types to meet the environmental demands of military applications.

* The Navy should encourage the development of new analog I/O processors by funding increased bandwidth and digital input capability of current devices. Currently available analog I/O processors are sufficiently fast to handle typical avionics control needs, but not fast enough for desired analog I/O processing. Analog I/O processor chips currently available have bandwidths in the 4 to 25 kilohertz range for typical applications of voice and other signal processing.

* A standard assembly language (SAL) is necessary to create the portability of ADA from computer to computer and eliminate the need to develop a new compiler for each new processor. An ADA compiler that produces a standard assembly language as an output should be developed. Current software standards (such as MIL-STD-1679) do not explicitly address the needs and requirements for interrupt driven systems, nor do they address the

documentation requirements for embedded signal processors. Amended standards discussing these and other special areas of embedded computer control should be addressed.

* Logical devices to be implemented by the VHSIC program might be the central processor units of the AN/UYK-43 and -44. The software development tools required to support these processors using existing languages are being developed as modifications to current Navy Standard Support Software Packages. The development of ADA software for these two processors should be an outgrowth of planned software tools for the existing standard computers.

* The Navy should also consider the development of algorithm libraries which address commonly recurring problems and make the libraries available to all potential users of the language. This goal can be realized by the production and distribution of manuals, magnetic tapes, and other media containing the libraries.

* Guidelines and procedures should be developed to promote better documentation of the technical, provable and operational aspects of embedded microcomputer systems software.

* Software management practices will have to be implemented in the development stage of an avionic system's life cycle. The imposition of software management controls without adding significant inefficiencies, removing incentives, or stifling innovation must be investigated. The configuration control of software will be a cost benefit to the Navy.

* The greater integration of discrete devices on one silicon chip allows integration of not only the processor, but also the inclusion of significant amounts of RAM and ROM. The inclusion of on-chip interpreters in human-interfacing applications will mean greater reliability of software action and lower parts count in the various implementations. The Navy should investigate the use of standard speech producing IC's to provide an indication of proper equipment operation or failure. The uses for speech are in combat as well as test environments. A possible area of development could be the coordinated presentation of speech and display information to a pilot or navigator in aircraft guidance or target acquisition and destruction. This combination of sensory input may not be realizable in the next few years, but independent development efforts should be made with implementation to be addressed in the 5 to 10 year time frame.

* Program verification will be eased in the near and long term efforts by the use of standard verification tools. As the tests will be performed in only one or two languages (ADA and CMS-2), the production of standard verification tools will be more easily implemented. The development of these tools may take 10 years, but the use of in-circuit emulators in the near term will allow formalization in documentation of the designed software systems.

* Current capabilities will grow in circuit density and speed.

* Software production may be aided by the creation of instruction set architectures which directly execute algorithms coded in ADA. An "ADA Engine" is being developed in the commercial world now and should be available to the Navy in the future.

* Signal processors will grow into array processors, with the capability of multi-dimensional processing in the analog and digital domains.

6.3.5.5 Development Priorities

Standards and/or guidelines must be further developed with respect to software design, documentation, validation, operation and maintenance.

An interface structure for embedded microcomputer systems must be defined and standardized.

Libraries of ADA written routines should be created and documented.

Training of personnel with respect to software development techniques, guidelines, standards, and languages should be undertaken.

6.3.5.6 Summary

Embedded microcomputers will become commonplace in avionics systems. The resulting designs will be more reliable, sophisticated, and faster. However, to achieve this end in a maintainable and cost effective way, it is necessary to establish both hardware and software standards in the immediate future. While the VHSIC program will help to attain hardware goals, significant implementation is several years away.

6.4 INSTRUMENTATION/CONTROLS/DISPLAYS

Navy tactical aircraft include control and display systems that are characterized by technology obsolescence, reliability and maintainability problems, and high support cost. The anticipated mission scenario of the next decade requires that the crew be presented with easily interpreted real-time information related to multifunction missions. The crew must then assimilate these data and quickly react to specific threats under conditions of high stress. Existing control and display systems are inadequate to alleviate the crew's peak workload, and do not provide the flexibility required to cope with the projected sophisticated missions of the future.

The crew must be provided with improved displays which have the necessary multi-mission, multi-mode and multi-level capabilities. The possibility of using universal modularized displays in future new aircraft and CILOP applications with bus structured avionics systems holds promise for impressive gains in capability, reliability, maintainability, and cost reduction,if innovative systems engineering and long range planning are accomplished in a timely manner. The following articles describe current control, display, and instrumentation equipment developments.

6.4.1 INTEGRATED MULTIFUNCTION CONTROLS AND DISPLAYS

6.4.1.1 Background

The requirements for increased mission capabilities, improved performance and expanded flight envelopes of today's military aircraft have placed stringent demands on the crew station designers to provide this performance within critically limited cockpit space and equally critically limited funding. These demands must be satisfied while simultaneously maintaining relative simplicity and ease of operation by the pilot.

The military has been a pioneer in the development of multifunction displays and controls for airborne use. All three services are attempting to integrate the display and control function by reducing and hopefully eventually eliminating all single purpose displays and controls, except where safety factors override.

6.4.1.2 Current Capability and Identified Deficiencies

Up to the 1970s, the transfer of information, with a few isolated exceptions, has been through use of moving mechanical devices and incandescent light bulbs, each serving a single function. This meant that even though it was used as low as 0.1% of the flying time of the aircraft, it was physically there taking up instrument panel space, panel depth, adding weight, consuming power and adding heat (which required more cooling air). If a failure occurred, there was no alternative location in which the lost information could be presented. More and more CRTs were added to the systems, first as radar screens, then as sensor displays and, finally, for computer generated imagery of weapon system parameters. As the weapon system complexities increased, more mechanical elements and light bulbs were added until the physical limitations of the cockpit were exhausted. The F-18 was the first successful attempt to have a truly integrated multifunction control display system. The Air Force's F-111 attempt in the early 70s was not considered successful because the state-of-the-art in electronics was not sufficiently advanced.

A similar look at the transfer of information from the man to the machine results in a similar conclusion. Toggle switches, pull handles, rotary and pushbutton switches were added as functions where required until, there too, no more panel space was available. Each panel, for each individual function, was there 100% of the time even if it was used 0.1% of the time. And if it failed, with very few exceptions, there was no alternate way to perform that function.

The electromechanical instruments presently used by the thousands in today's aircraft exhibit a number of deficiencies:

* Complex interfaces between the analog devices and the digital systems are required.

* Poor reliability due to the wearing out of moving parts is experienced.

* Poor maintainability due to the skill level required is attained. (Boeing, on their 757/767, aircraft series, will use all multifunction displays because they believe that by the year 1990 the "watchmaker" type of skills presently required to repair dedicated electro mechanical instruments will have almost disappeared, thereby driving maintenance costs to exhorbitant levels.)

In order to explore the deficiencies of multifunction displays, it is necessary to understand what multifunction displays will be required. A Tri-Service Working Group has established the following four major types:

The Head-Up Display (HUD) is a collimated (focused at infinity), optically projected display designed specifically for airborne use. The HUD combining glass is located between the aircraft windscreen and glare shield and functions as an optical beamsplitter. The combiner/beamsplitter transmits the real-world scene directly and reflects the display image so that the pilot views the two superimposed images simultaneously. The HUD's field of view (FOV) is scaled to be the same as that of the real-world scene. Because the reflected image is collimated, the angular size and position of symbol cues projected within the display FOV remain constant with pilot head motion. The HUD is used to project vector-graphic or video information. The HUD's primary functions are weapon-aiming and flight control; therefore, a high-quality optical system is required to maintain accurate symbol positioning over the entire display FOV. The HUD also displays symbol cues for other mission modes such as takeoff, landing navigation, and terrain following/avoidance. Electro-optical sensor displays such as forward-looking infrared (FLIR) can also be presented on the HUD.

The Helmet-Mounted Display (HMD) is a collimated (focused at infinity), virtual image display that is mounted to, or built integrally with, the pilot's flight helmet. The image is generated on a miniature image source with a display size of typically one inch. The image is relayed from the miniature image source, usually mounted somewhere on the helmet, through an optical system, also on the helmet, to a point where it is projected via a final beamsplitter on the visor into the pilot's eye. The pilot sees a virtual image of the displayed information, in his forward field of regard, superimposed over his view of the real world. Thus, the pilot can always see the entire display and does not have to look at the instrument panel, or to look forward through HUD, to have access to the display. The typical FOV of the HMD would be equivalent to having a large (21-inch diagonal screen) television display in the cockpit. The HMD presents a variety of different types of information and is used primarily to present high-resolution video imagery from the FLIR, daytime, and low-light-level TV sensors onboard the aircraft. This type of information is used to pilot a vehicle, for target acquisition, weapon delivery, navigation, and terrain avoidance aspects of the mission. The HMD is also used to present a variety of different types of symbology. These range in complexity from simple gunsight reticles and discrete cues to flight-control and navigation symbology typical of head-up display presentation, complex stabilized weapon delivery symbology, and vector-graphics. In short, the type of information being presented by the HMD system can cover the full gamut of information presented by any of the other cockpit displays.

The Multipurpose Display (MPD) is a direct view, flexible information format display that can display both graphic and video information. It allows the aircrew to both monitor and exercise real-time control over the aircraft and its related systems. The MPD may also serve in failure backup mode as a display for information generally found elsewhere in the cockpit. Depending on the control-display requirements assigned to a MPD, it can either perform all the primary flight display functions in the cockpit, or alternatively, just a portion of them. The Horizontal Situation Display (HSD) and the Vertical Situation Display (VSD) are two classes of MPD that are associated with two specific types of flight control display information. The HSD is a flexible information format (that is, multifunction) display that, as a minimum, displays the heading information portrayed on a conventional electromechanical horizontal situation indicator (HSI) or a radio magnetic indicator (RMI). In essence, it is a MPD that has a designated information function: it displays information which gives aircraft orientation and any related situation information with respect to a position in a plane horizontal to the earth's surface. In addition to the heading indication, bearing pointers, distance, and course deviation indication provided by an HSI, the HSD should be able to provide combinations of:

* Aeronautical charts and/or electronically generated maps,

* Navigation, target drop zone identification,

* Electro-optical and radar sensor video,

* Flight control cues, and

* Electronic warfare information.

The VSD is a flexible information format (that is, multifunction) display which, as a minimum, displays the attitude information portrayed on an electromechanical attitude director indicator (ADI). The VSD is also a form of MPD that has a designated function to display the following kinds of information:

* Electro-optical and radar sensor video,

* Target acquisition and identification sensors,

* Weapons delivery, and

* Caution, warning, and advisory annunciation.

The Mission Management Display (MMD) is a flexible information format display which portrays and permits interactive control of high information content, computer-generated alphanumeric and graphic information. Two basic units are envisioned, a monitor control display (MCD) with relatively high resolution (100-120 pixels/inch), and a data management display (DMD) with relatively low resolution (50-80 pixels/inch). The MCD is a high-performance display that can portray computer-generated vector-graphic aircraft situation data, including moving symbolic map, three-dimensional perspective, contact analog, terrain-following contour map, flight control, and other high-update-rate information. The DMD portrays aircraft-related

subsystems data such as engine, fuel, hydraulic, oxygen, and life-support systems information; ordnance data such as weapon type, status, and readiness; and avionic subsystem modes and status such as navigation, communication, electronic support measures (ESMs) and countermeasures, sensors, and processing. Each type of information is prioritized for automatic presentation for each mission mode so that the most important data at the particular moment during a mission receive the highest attention. The information is also available by operator command. Note that the MMD does not have the capability to display video information.

At the present time, CRTs are used for three of the four applications. The CRT is a very flexible device that is normally credited with the following deficiencies:

* Depth is normally at least twice the height of the viewing screen. This not only presents a problem in new aircraft in allowing space behind the panel but is prohibitive in retrofitting older aircraft (especially rotary wing) where space is not available.

* Adjustments are required periodically for focus and linearity (convergence adjustment may be required in future color systems).

* Power required for the deflection voltages (12,000 to 18,000 volts) present difficult supply design problems. Power supply failures and degradations are the prime causes of display failures and not the CRT itself.

Specific problems for each application are as follows:

HUD:

* Brightness requirements, to be viewable against a 10,000 ft-lambert ambient, present the biggest deficiency for the HUD.

* Depth problems are increased due to the addition of optics for collimation. The physical problem is the "waste" of prime instrument panel real estate which, up to now, has been wasted or covered as a "band-aid" by a control panel which could not be placed in the consoles due to lack of space.

HMD (Same as HUD):

* Weight added to the helmet induces a fatigue problem which is compounded in High-G aircraft if the center of gravity is shifted such that neck injuries are possible.

* Dynamic range requirements to allow between 8 to 16 shades of gray in high ambient light conditions are not available on a consistent basis, due to life time degradations.

There are no SAD displays being used with CRTs because the cost effectiveness of using a CRT for this single group of specialized functions would be prohibitive. However, relatively inexpensive flat panels of the future would allow the inclusion of this type of display in advanced weapon systems and retrofit into existing systems as they are proven.

Currently, electromechanical controls have the following deficiencies:

* Inflexible - they cannot be easily modified and do not lend themselves to being integrated, since they are mostly single function devices.

* Reliability - poor due to their mechanical nature.

* Sensing - nearly impossible, if not impractical, such that performance monitoring is non-existent.

Attempts have been made to make multifunction controls, but problems have developed:

* The F-14 aircraft has a revolving drum with legends imprinted on it, which is surrounded by switches. The moving parts present reliability problems and the imprinted legends are inflexible and expensive to change.

* The F-18 uses incandescent bulbs in the up-front control panel, which have a reliability and heat problem as well as a viewability problem in high-ambient light conditions. The F-18 also uses the MPD CRT perimeter to present legends keyed to switches surrounding all four edges of the CRT. This has been favorably received except that more and more legends are required, which steals more and more lines of video since the legends are presented in a stroke mode during the retrace time.

* The LAMPS MK III aircraft has an acoustic noise problem caused by the fan required to remove excess heat from incandescent bulbs, and difficulty has been experienced in modifying the engraved legends.

The Tri-Service Working Group has identified the Multifunction Programmable Keyboard (MFPK) as a fifth type of unit.

The Multifunction Programmable Keyboard (MFPK) is an array of switches whose legends can be changed under software control through pilot interaction. This can be implemented with either individual switches or one panel with touch capability. The MFPK can integrate the control of several sets of functions presently provided by separate/dedicated control panels and the management of several primary multifunction displays. It can reduce operator real-time workload both by allowing preselection of flight tasks on a functional or mission-segment basis and by providing flexible, but orderly, procedures in the conduct of the total crew station management. Through the

use of the MFPK, the multitude of dedicated control switches can be sharply reduced and I/O cueing, heretofore not available, can be provided. The use of flat panel technology will make this possible.

6.4.1.3 Equipment Development and Modernization

The Navy, in advanced development, is attempting to solve the previously described deficiencies (and others) through a program called AIDS (Advanced Integrated Display System).

AIDS is basically a three-pronged approach:

* Advance technology,

* Advance system integration concepts, and

* Advance human factors concepts.

An attempt is being made to improve the man-machine information transfer by the basic philosophy of "keep it natural". This means that the man-machine information transfer should be as similar as possible to a man-man information transfer which includes voice-interaction, extensive use of color coding, extensive use of pictures vice words and presentations of alternative and recommended solutions vice data.

Advanced technology for displays and controls can be further subdivided into the following areas:

* Display Surfaces,

* Electronics, and

* Graphics Software Development.

The last two items shall not be covered here except to say that the future Display and Control Systems are dependent on ongoing parallel developments.

Display Surfaces developments are required for the CRT and for Flat Panels.

CRT improvement requirements include more efficient guns for monochrome displays and improved phosphors, screens and power supplies for color displays.

In the system integration area, AIDS makes extensive use of modular construction, a bus concept utilizing MIL-STD-1553 for digital transmission and a video bus for the transmission of pictorial information, whether it be sensor or computer generated. This greatly simplifies the design, implementation, repair and future modification of the system in that two buses connect the avionics bay with the cockpit (digital and video). A second set of redundancy greatly enhances the reliability, probability for mission success and maintainability.

At the present time, many flat panel technologies are being pursued. Three candidates; Electroluminescent (EL), Light-Emitting-Diodes (LED), and Liquid Crystals (LC) all appear to be promising for airborne applications. Each has advantages and disadvantages. At the present time, it does not appear that any single technology can satisfy all applications. It is recommended that development continue as shown below:

	EL	LED	LC
HUD			X
HMD	X		X
MPD	X	X	
SAD	X	X	X
MFPK	X	X	X

6.4.1.4 Summary of Requirements

Short Term (0 to 5 years) - This time period will also only be concerned with retrofit of existing aircraft with CRT HUD, MPD and MFPK where space will allow.

Mid Term (5 to 10 years) - This time period will be concerned with retrofit of existing aircraft, but will also include a CRT HMD and flat panel SAD and MFPK. (Voice interaction will also be introduced with voice synthesis.)

Long Term (10 years plus) - This time period will not only include retrofits, but also new weapon system developments in VSTOL and longer range aircraft which should include fully integrated systems using Flat Panel HUD, HMD, MPD, SAD and MFPK. (Voice interaction will be heavily involved with both voice synthesis and voice recognition.)

6.4.1.5 Development Priorities

The priorities for the Integrated Multifunction Displays and Controls should be:

* Flat panel development for:
  * SAD and MFPK
  * HMD
  * HUD
  * MPD
* Video bus for color and high resolution (875-1024 line)
* Programmable raster symbol generators having high speed computational power for 3-D graphics

6.4.2 CONTROLS AND DISPLAYS FOR THE F/A-18

6.4.2.1 Background

In the mid 1970's, the Navy set out to develop and produce a low-cost, light weight, high performance, multi-mission fighter. Early in the program development, it became clear that an efficient, integrated cockpit was needed. The resulting design has greatly improved the man-machine interface by use of multiple computer-aided displays and controls. This efficient, space saving cockpit, along with a high degree of automation, will considerably reduce the pilot's workload, thus enabling him to both maneuver the aircraft and operate the weapons system in combat situations.

6.4.2.2 Current Capability

The Fighter/Attack (F/A)-18 cockpit has been optimized for one-man operation and incorporates multi-function Cathode Ray Tube (CRT) displays that minimize operator controls. Two of three identically sized five-inch indicators are positioned high and to the sides of the cockpit front panel. One of these, the Multifunction Display (MFD), is the primary sensor display for radar-attack mapping, forward-looking infrared (FLIR), and electro-optical sensors. Superimposed on the sensor data are other aircraft data, including weapon status and other alphanumeric symbols. The Master Monitor Display (MMD) occupies the other Head-up position, and is the primary warning, built-in-test, armament, and general purpose display. In a centered, head-down location position (to prevent sunlight intervention) is the Electronic Horizontal Situation Indicator (EHSI). This display presents plan view navigation information, along with other visual aids. In the A-18 version, the EHSI is replaced by a Horizontal Situation Display (HSD) that superimposes the electronic CRT symbology over a projected color map display. The F/A-18 Heads-Up-Display (HUD) is the primary flight instrument for navigation and weapon delivery. All essential flight data are also displayed on the HUD. Reliability is enhanced through the use of redundant display generators and interchangeable display functions. Controls in the F/A-18 are minimized through the use of programmable functions. Push buttons are positioned around the periphery of the multimode displays, enabling the function of the button to be indicated next to the button. An Up-Front-Control (UFC) panel positioned in the center head-up position of the cockpit has been provided for Communication-Navigation-Identification (CNI) functions. The UFC panel has a programmable alpha-numeric display with adjacent multi-function switches. To aid the pilot with his formidable tasks during combat situations, the F/A-18 has adopted a Hands-On Throttle and Stick (HOTAS) concept allowing the pilot to control weapons, sensors and displays.

6.4.2.3 Equipment Development and Modernization

The F/A-18 cockpit controls and displays developments have resulted in a system that is flexible enough to accomodate growth. Modernization and development efforts for other aircraft will capitalize on these capabilities.

In an effort to further free the pilot from physical console activity, voice recognition capabilities may be integrated with the controls and displays. This would be especially useful for entry of numbers such as radio channels and frequencies and navigation headings.

The VHSIC digital logic and Very Large Scale Integration (VLSI) components will make possible implementation of powerful display processors capable of advance real-time graphics, real-time image processing and enhancement, and real-time registration and alignment of multiple sensor sources or stored images to generate overlays. A development program should be structured to provide a multi-aircraft display system with evolutionary growth potential through modular implementation and standardized interfaces.

Displays for engine/aircraft performance monitoring are another candidate for improvement. Digital numeric displays require considerable conscious effort to use. A demonstration of display formats that overcome this drawback is planned.

6.4.2.4 Summary of Requirements

Short term (0 to 5 years) -

* Develop an integrated voice recognition capability.

* Develop a display system architecture with standardized wide bandwidth interfaces and the capability to manipulate sensor or stored images.

* Develop improved displays and display formats for engine/aircraft performance data.

Mid Term (5 to 10 years) -

* Integrate voice recognition techniques into the F/A-18.

* Plan and develop a phased update of display system components and functions to include transition interfaces.

Long Term (10 years plus) -

* Implement modular, completely integrated displays/controls/information system.

6.4.2.5 Development Priorities

Since voice recognition capability could greatly enhance efficiency and the F/A-18 may be easily adapted to use it, this effort should be given high priority. Beyond this, a sustained program of integrated display system development should be undertaken to develop systems for all Navy aircraft need, and to apply the lessons learned from the F/A-18, Navy Advanced Integrated Display System (AIDS) and Air Force Digital Avionics Information System (DAIS) programs.

6.4.3 CONTROLS AND DISPLAYS FOR LIGHT AIRBORNE MULTIPURPOSE SYSTEM (LAMPS) MK III

6.4.3.1 Background

Modern technology has produced faster and quieter submarines, able to cruise thousands of miles without surfacing. Therefore, the Navy's anti-submarine warfare program required new sensors and processors to detect, classify, localize, and attack this threat. The LAMPS MK III Air/Ship system has been developed to satisfy these requirements.

6.4.3.2 Current Capability and Identified Deficiencies

Controls:

The AN/ASQ-164 Control-Indicator Set (keysets) provides the primary interface between the LAMPS MK III avionics system, the Airborne Tactical Officer (ATO), and the Sensor Operator (SO). The keysets provide functions for the operators to transmit and receive information and a force stick for control of cursor position on the ATO and SO cathode ray tube (CRT) displays.

The keysets allow the ATO and SO to communicate with the AN/AYK-14(V) Standard Airborne Computer via the LAMPS MK III avionics MIL-STD-1553 system data bus. Each keyset switch can be illuminated to indicate one of three status categories:

Illumination State	Meaning
Blank	Switch function not available to operator
White	Switch function available to operator
Green	Switch function activated by operator

The ATO and SO keysets are electrically and mechanically similar. SRA's for each keyset are identical, except for the front panel interface printed circuit card.

The keysets employ low power Schottky technology. Additionally, each keyset contains a microprocessor dedicated solely to Built-In-Test (BIT) manipulations.

The keysets now in use were designed as part of the LAMPS MK III full scale development system currently undergoing Navy preliminary evaluation testing. Deficiencies identified to date are:

* Difficulty in replacing front panel components.

* Excessive acoustic noise generated by cooling fan.

Displays:

The CV-3252/A converter-display is utilized by the LAMPS MK III avionics system to provide the ATO and SO with presentations of tactical, navigation, and sensor data.

The converter-display is a self contained equipment using a CRT to produce the display images. The converter display operates in a symbol mode or raster mode or both, through the use of time-multiplexed input signals. The symbol mode display depicts the tactical and navigational situation and is also capable of presenting information by alphanumerics in either tabular or text form. The raster mode is capable of displaying sensor equipment information. All information for the converter-display is processed by the LAMPS MK III converter-multiplexer (CMUX), CV-3435/A.

The primary deficiency of the converter-display is that it is totally dependent on the CMUX for display information. All converter-display capability is lost in the event of a CMUX failure.

If a CMUX failure were to occur, no radar display would be available to the ATO and SO because radar information from the radar signal data converter (SDC) is processed by the CMUX for presentation on the converter-display. Since radar capability is critical to navigation, a back-up capability to process and display radar information from the SDC should be added to the converter-dislay.

6.4.3.3 Equipment Development and Modernization

Controls:

The AN/ASQ-164 control-indicator set was developed specifically for the LAMPS MK III program. All reliability, maintainability, and environmental testing of the keysets has been completed. A product improvement program has begun for production keysets. Areas addressed in the program include:

* Use of a microprocessor to control internal logic functions, thereby reducing parts count/power requirements and the number of printed circuit cards while increasing error detection capability and improving reliability.

* Utilization of an integrated MIL-STD-1553 data bus I/O chip, allowing a reduced component count.

* Incorporation of simple, modular switch arrays which allow improved switch reliability, simplified front panel assembly, maintenance procedures, and identical switch modules with easily replaceable switch legends.

* Redesign of the power supply to reduce parts count, increase efficiency, and improve reliability.

* Use of a slower speed fan to reduce acoustic noise level.

* Requalification of the new design.

Displays:

The CV-3252/A converter-display was developed specifically for use in the LAMPS MK III avionics system. However, since it is a general purpose display, consideration should be given to using the converter-display in other systems.

While the cathode ray tube has proven capabilities, consideration should be given to newer display technologies. Solid state displays, plasma displays and liquid crystal displays with electroluminescent backlighting show promise as possible replacements for CRT displays.

6.4.3.4 Summary of Requirements

Short Term (0 to 5 years) -

* Controls
  * Implement a product improvement program for production keysets.
  * Investigate the feasibility of incorporating software definable multiple function switches to reduce switch count.
* Displays
  * Include a backup radar display capability for LAMPS MK III.
  * Investigate the use of CV-3252/A converter-display in other systems.
  * Investigate new display technologies.

Mid Term (5 to 10 years) -

* Controls
  * Incorporate the multiple function switches.
* Displays
  * Incorporate the CV-3252/A into new systems when applicable.
  * Incorporate newer display technologies, if viable.

Long Term (10 years plus) -

* Controls
  * Study alternate data entry schemes (e.g., voice entry).
* Displays
  * Phase out CRT displays with newer technology where practical.

6.4.3.5 Development Priorities

* Implement a product improvement program for production keysets.

* Include a backup radar display capability in LAMPS MK-III.

6.4.3.6 Ongoing Programs

The product improvement program for the LAMPS MK-III Control-Indicator Set was established to increase reliability and maintainability while reducing system complexity and cost.

MILESTONES

FY 81	
Critical Design Review	Jan 81
Complete Software Debug	Apr 81
Start Fabrication	May 81
Begin Bench Test	Aug 81
Begin Environmental Qualification Test	Sep 81
Start Reliability Demonstration Test	Sep 81
FY 82	
Perform Maintainability Demonstration	Oct 81
Lot I Production Go-Ahead	Oct 81
Complete Environmental Qualification Test	Oct 81
Complete Reliability Demonstration Test	Apr 82
FY 83	
Complete Production of Lot I Keysets	Oct 82

6.4.4 VOICE RECOGNITION AND SYNTHESIS (VRAS)

6.4.4.1 Background

The large number of different systems that must be managed by an aircrew to accomplish a complex mission poses a difficult problem for the crew station designer. As new sensors, weapons, and CNI equipments are incorporated into the avionics suite of an emerging system, the crew station becomes progressively more crowded by manual controls and visual displays. Current solutions to this problem rely upon multipurpose controls and displays, and a variety of aural alarms. Multipurpose control sets make it possible for the crew station designer to place all relevant controls and displays for several subsystems directly in front of the operator, but they aggravate the problem of operator workload in their continued reliance on the operator's visual/manual information channels.

The general objective of the Voice Recognition And Synthesis (VRAS) effort is to resolve the problem of excessive visual/manual workload in naval avionic systems by developing a capability to transfer visual and motor operator tasks to the less saturated vocal/auditory input and output modes. This requires: (a) demonstration of the applicability and effectiveness of voice

recognition, processing, and synthesis technology in the performance of complex operator tasks in airborne systems, and (b) the definition of detailed specifications for the integration of voice systems hardware and software into airborne systems.

Several operator/hardware/software configurations are being developed and tested in simulator and flight-test platforms at the Naval Air Development Center (NADC), Naval Training Equipment Center (NTEC), and the NASA-Ames Research Center. These systems are being exercised to derive cost/performance trade-offs and to generate detailed hardware, software, and human engineering specifications.

6.4.4.2 Current Status

There is presently no voice recognition capability implemented in Fleet combat aircraft. Preliminary data indicate that operational voice-interactive systems are technically feasible, and will provide crew station designers with a powerful alternative to conventional display and control technologies. Several studies have shown that voice systems obviate many controls and displays in crew stations, and effectively augment others, resulting in improved utilization of human operators. Voice systems have been successfully integrated into training systems, resulting in reduced instructor/student ratio. A new thrust in FY-81 will explore the use of voice technology for training maintenance personnel and in the design of maintenance systems.

Although the primary thrust of the VRAS project is to develop voice-controlled avionic systems, the underlying technology is applicable to all manned platforms, and many maintenance and training systems. Specific users of products developed under this project include: (a) the Advanced Integrated Display System (AIDS) program at NADC; (b) Flight Performance Enhancement program at NADC; (c) Naval Underwater Systems Center (NUSC), New London, CT; (d) NUSC, Groton, CT; (e) NTEC; (f) Air Force Flight Dynamics Laboratory; (g) NASA Ames Research Center.

6.4.4.3 Perceived Trends

As a consequence of aircraft multimission requirements, avionics system reconfiguration requirements, avionics control/status complexity, and the limited skills maintenance personnel, the trends are favoring approaches which address and allow for more simplified operation and maintenance routines. Avionics control/status systems which now utilize manual integrated control/status panels and/or automatic computer control/status activation will be replaced in an evolutionary manner by voice activation. The evolution has already begun within military aircraft via the incorporation of speech warning systems. For those aircraft which incorporate the MIL-STD-1553B Data Bus System, speech technology can be incorporated via data bus access in terms of MIL-STD-1553B protocol Command/Data and Status/Data words. As speech technology matures in terms of intelligibility, size of vocabulary, and noise rejection, it can begin to substitute speech commands for manual control/status actions and synthesized voice status indicators. The data bus system can provide the interconnectivity vehicle for the accommodation of this technology on an evolutionary basis. This trend is becoming more and more apparent as avionics and airframe manufacturers address the problems of complex and sophisticated system control and maintenance.

AD-A097 522 NAVAL AIR SYSTEMS COMMAND WASHINGTON DC F/G 9/5
NAVAIR AVIONICS MASTER PLAN.(U)
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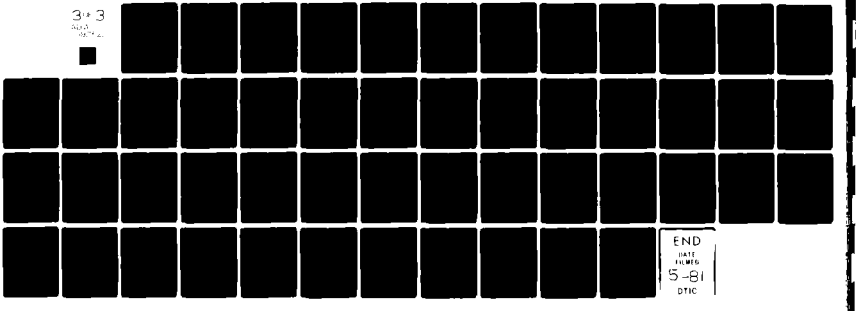

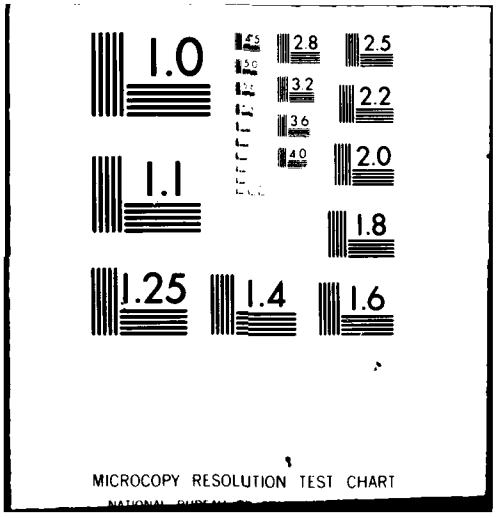
1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
MICROCOPY RESOLUTION TEST CHART

6.4.4.4 Areas Requiring Further Development

The general thrust of the VRAS program is to develop and validate voice-controlled avionic systems. Applications for voice recognition systems must be carefully identified and one or a family of reliable voice recognition algorithms usable in a military noise environment must be developed. Aircrew workload analyses must be accomplished and an estimate of the workload reduction achievable must be made. The reliability and dependability of the system and any impact on aircraft safety must be evaluated. The need for redundant backup systems must be evaluated. The impact of VRAS systems on avionic system weight, size, and power consumption must be estimated. Some of the in-house and contractual efforts tentatively planned for FY 82 reflect this goal. However, the significant expansion in the commercial/industrial technology base that has occurred in the last several months suggests that the original project goals are relatively narrow. That is, the methodologies and systems developed under this effort could be used to address problems in the design of other types of systems. In response to these developments, future studies will address applicability of voice technology to design of maintenance systems, and the training of maintenance personnel.

6.4.4.5 Development Priorities

Initiate/continue developments in the following areas: (a) development of a methodology for the comparative evaluation of speech recognition systems; (b) implementation, integration, test and evaluation of VRAS systems with advanced control/display panels and development of MIL-STD-1553B data bus interface components in navy avionic system development laboratories such as the NADC BASIC laboratory and the NAC DASL laboratory; (c) evaluation of F-14A, F/A-18A, and P-3C (III) platforms to define potential voice display/control functions; (d) flight testing of commercial/industrial speech recognition and synthesis systems; and (e) planning of a DOD/Industry mini-symposium on airborne applications of recognition/synthesis technology.

Products of these efforts will be data and methods that are summarized in various technical reports, and reconfigurable test systems that are used to develop detailed functional and engineering specifications for airborne voice-interactive systems.

6.4.4.6 Summary

The demands placed on crew members of high performance aircraft have resulted in near saturation of the traditional visual and motor channels. A method of using alternate sensing and control channels is required to relieve this overload; Voice Interactive Systems (VIS) offer such a capability.

VRAS is part of a coordinated exploratory and advanced development program entitled "Voice Interactive Systems and Technology." The objective of the program is to develop an airborne voice interactive system that will permit a crew member to obtain information, or change system status, with voice requests or commands. The final product of the program will be a conclusive test of the feasibility of such systems.

The exploratory development component of the program addresses the following areas: (a) development of Limited Continuous Speech Recognition (LCSR) technology; (b) development of voice annunciator technology; (c) development of data and methods that can be employed in the analysis of existing or emerging aircraft crewstations to determine suitability and specific functions of voice systems; (d) analysis of candidate applications in weapon system trainers, and in design of maintenance aids/systems, and (e) development of methods for test and evaluation of voice systems.

6.4.5 AIR DATA COMPUTERS (ADCs)

6.4.5.1 Background

The Air Data Computer (ADC) converts raw air data inputs into highly accurate electrical outputs which are used for flight reference, navigation, and weapons release functions. The air mass inputs to the ADC, i.e., total temperature, static pressure, pitot pressure, and angle of attack, are used to develop barometric altitude, mach number, true angle of attack, true airspeed, indicated air speed, and derivatives thereof. The outputs developed by the ADC are displayed on instruments located in the cockpit and routed to other avionics systems that require precise air data information, such as weapon release, IFF transponder, navigation, engine performance, radar, environment control, wing sweep, warning indicators, and autopilot.

6.4.5.2 Current Capability and Identified Deficiencies

The majority of the ADCs in fleet use are electromechanical devices of 1960 vintage which are difficult to maintain (high scheduled/unscheduled maintenance times due to time consuming alignment procedures), exhibit poor reliability [the Mean Flight Hours Between Failure (MFHBF) average less than 90 hours, the Mean Flight Hours Between Maintenance Action (MFHBMA) average less than 50 hours], have faulty performance (in both flight safety and weapons delivery accuracy), and require extensive logistic support (due to high parts count of each computer). Each Navy aircraft type has a unique ADC, although all perform the same basic computations. There have been 52 unique ADCs developed since 1958, of which approximately 27 types (approximately 3600 total units) are still used in the fleet. Current military designs for the F-14, F-18, and AV-8B aircraft provide a mature technology for developing digital ADCs which are more reliable, easier to maintain, and which have lower logistic support costs than the present analog and early digital ADCs.

Current helicopters are equipped with a pitot-static airspeed system that is unidirectional and unreliable at airspeeds less than approximately 55 knots. The pitot-static airspeed system cannot accurately determine airspeed when operating in close proximity to the ground/water, cannot provide the pilot with wind direction and velocity required for safe rotor engagement/disengagement when operating in high wind conditions, or provide a means of determining when the lateral and rearward flight envelope are being exceeded, and does not permit maximum utilization of the helicopter. The current airspeed system thus poses a potential hazard to safe operations.

The present method of acquiring ADCs is to procure them as part of the total airframe; i.e., as Contractor Furnished Equipment (CFE). As a result, each aircraft has a functionally similar, yet logistically unique ADC.

A major concern among the military avionics community is the growing life cycle cost (LCC) of unique avionic equipments that increase with each new aircraft development. Because of the small quantities associated with any particular aircraft, the result is a growing cost burden in the areas of development, procurement, logistics and maintenance. A comprehensive and methodical approach to reduce proliferation is possible by developing standard ADCs for common application to multiple aircraft types.

6.4.5.3 Equipment Development and Modernization

A standard ADC that combines the requirements and functions of 11 existing ADCs into a single unit is being developed primarily to replace the current population of unreliable ADCs and, at the same time, have the capability to be forward fit into new production aircraft as future requirements are defined. The goal is to develop a cost effective ADC which has direct interchangeability with current equipment. Initial ADC applications are for the A-4M, EA-6A, EA-6B, KA-6D, A-6E, A-7E, TA-7C, E-2C, C-2A, AND VCX aircraft. Incorporation of the ADC in the F-4 and F-14 would probably be concurrent with other avionics modifications. Provision for a MIL-STD-1553B digital multiplex data interface will be required for new aircraft and CILOP aircraft.

The development will provide a modularized ADC which has an upper test Mean Time Between Failure (MTBF) of 1600 hours and a lower test MTBF of 800 hours. The design will feature Built-In-Test (BIT) to accomplish failure detection without the assistance of Ground Support Equipment (GSE) at the Organizational (O) Level. The need for test equipment for Intermediate (I) Level isolation to a Shop Replaceable Assembly (SRA) will be minimized.

The objectives of the ADC development are to provide an ADC which is reliable; reduce ILS cost by developing, through Approval for Service Use (ASU), common ADCs for application to multiple aircraft types; and, provide a validated data package which can be used to support competitive procurement of large production quantities.

The ADC development is a coordinated Navy/Marine Corps/Air Force program. A joint Navy/Marine Corps/Air Force performance specification has been prepared and reviewed by industry/government. The plans are to retrofit approximately 2000 Navy/Marine aircraft with standard ADCs. Air Force requirements could add another 3200 units.

MILESTONES

Issue Solicitation (RFP)	Mar 81
Contracts Award (Development)	Sep 81
TECHEVAL/OPEVAL	Mar - Dec 83
ASU	Feb 84
Contract Award (Production)	Mar 84

Two additional ADC developments are currently in process. Development of an F-18 ADC, which is an outgrowth of the ADCs developed for the F-15 and F-16 aircraft, began in November 1976. Navy flight tests began in January

1980, and the ADC has demonstrated high reliability and accuracy. A development contract was awarded for an AV-8B ADC in early FY 80. Limited production is planned for FY 83.

Various low airspeed and omnidirectional air data systems (ADSs) are under conceptual development. The ADS is to be used for all helicopters engaged in training and assault support combat missions. The ADS will permit safe utilization of the full capabilities of the helicopter; allow the use of new techniques and tactics for improvement of the helicopter as a weapon system and assault support vehicle; and, provide information to the pilot that will preclude unintentional operations outside of the aircraft flight envelope. The ADS will be capable of operation and storage in all climatic and all weather conditions. The ADS will provide omnidirectional readout capability of flight path airspeed or relative wind. It is desired that the system provide the same capability for V/STOL aircraft below 150 knots and be structurally capable of withstanding maximum V/STOL aircraft speeds.

Three existing ADCs have been redesigned under the auspices of the Aircraft Equipment Reliability and Maintainability Improvement Program (AERMIP) to provide a single analog ADC which is common to the EA-6A, EA-6B, and KA-6D aircraft. The design changes will reduce maintenance time, improve reliability and simplify logistic support. A retrofit contract is anticipated in January 1981.

6.4.5.4 Summary of Requirements

Short Term (0 to 5 years) - Short term efforts include:

* Develop a standard ADC for use in retrofit and CILOP applications.

* Evaluate gust indication and air temperature gradient parameters for possible inclusion in future ADCs.

* Award a production contract for retrofit of the EA-6A, EA-6B, and KA-6D.

Mid Term (5 to 10 years) - Mid term efforts include:

* Evaluate alternate systems to the pitot-static pneumatic system for air mass sensing.

* Evaluate the change from the parallel format of the AIMS code to a serial code. This would reduce aircraft wiring requirements for transmission of the AIMS output and allow use of a data bus.

* Develop a standard ADC pressure transducer.

* Develop a standard low-airspeed omnidirectional ADS.

Long Term (10 years plus) - Long term efforts include:

* Develop an all digital ADC that includes digital I/O. This would require that all interface equipment be compatible with the MIL-STD-1553 data bus.

6.4.5.5 Development Priorities

Development priorities are:

* Develop a standard ADC to replace the current population of unreliable analog ADC.

* Develop a standard low-airspeed omnidirectional ADS to permit safe utilization of the full capabilities of the helicopter.

6.4.6 FLIGHT INCIDENT RECORDERS

6.4.6.1 Background

Accident investigations concerning high performance military aircraft, such as tactical fighter-bombers and air-superiority fighters, are now severely hampered in determining the actual cause of an aircraft mishap due to the lack of information on aircraft parameters and flight conditions immediately preceding the event. Damage from impact and fire usually makes analysis of the remaining debris extremely difficult and often non-conclusive. Most high performance aircraft contain many complex subsystems which may contribute separately or in a combined manner to cause an aircraft mishap. The monitoring of critical performance parameters in each of these subsystems provides extremely valuable information for accident investigation. Access to this information after an accident requires that the data storage media survive virtually intact while retaining the stored parameter data.

Crash data recording systems used on commercial passenger carrying aircraft are not suitable for military high-performance aircraft because of excessive size and weight. In addition to these considerations, a flight data recording system must be sufficiently low in initial cost and designed for minimum logistic support costs to permit fleet-wide implementation. Data from 1975 to August 1980 indicate that 43% of all Navy aircraft crashes occur at sea. Based on this data, the Navy strongly supports the development of a FIR whose memory unit is deployable and floatable, and includes a crash position indicator.

6.4.6.2 Current Capability and Identified Deficiencies

The Recorder, Locator AN/ASH-20(V), the initial FIR developed for the Navy, was installed in Fleet aircraft (P-3B, E-2B, C-2A, and KC-130R) in 1971. During the development phase, little or no reliability testing or integrated logistics support planning was accomplished. The many failures of this system in actual crashes can be traced directly to low hardware reliability under crash conditions (primarily due to the magnetic tape recorder), and inadequate maintenance and logistics support.

In early 1978, NAVAIR began an intensive reliability and maintenance test program that resulted in extensive redesign of the AN/ASH-20(V) system. This program has resulted in a two-phase Engineering Change Proposal (ECP) to modify the AN/ASH-20(V) and to provide the much needed integrated logistics support.

6.4.6.3 Equipment Development and Modernization

Current NAVAIR planning delineates the requirements for a deployable FIR containing a non-volatile solid state memory. Both bubble and Metal Nitride Oxide Semiconductor (MNOS) memories are being investigated. The FIR is divided into three functional areas:

* Information gathering (audio, propulsion, navigation, etc.).

* Information transformation (analog to digital, MIL-STD-1553 Data Bus, conversion, level shifting).

* Information storage (memory).

The FIR development and packaging options including the use of Modular Avionics Packaging, are being assessed. A complete acquisition strategy will be defined in FY 82.

6.4.6.4 Summary of Requirements

Short Term (0 to 5 years) -

* Define FIR requirements and prepare an FIR performance specification.

* Develop FIR units based on the three functional area concept,

* Select and evaluate a non-volatile memory,

* Incorporate integrated logistics support requirement, and

* Introduce an improved solid-state FIR into selected Fleet aircraft.

Mid Term (5 to 10 years) -

* Develop the contracting strategy for production quantities,

* Introduce FIR into all Fleet aircraft, and

* Monitor and improve reliability and maintainability.

Long Term (10 years plus) -

* Provide reliability and maintainability improvements,

* Improve life cycle cost,

* Monitor technology advances, and

* Modify the FIR to improve operational performance.

6.4.6.5 Development Priorities

* Document FIR program policy,

* Determine aircraft parameters and audio data to be recorded,

* Prepare an FIR performance specification,,

* Select and evaluate a non-volatile, solid-state memory technology,

* Develop a deployable, crash survivable FIR package,

* Utilize a standard avionics module concept for FIR units, and

* Prepare a data package for support of low risk, competitive procurement.

6.4.6.6 Ongoing Program

MILESTONES

FY 81	
Determine aircraft parameters and audio data to be recorded, based on the inputs from CRAC, Navy Safety Center, and other Navy personnel.	Apr 1981
Review FIR parameter specification which will be prepared by NATC.	Continue
Prepare FIR performance specification.	Continue
Evaluate non-volatile, solid-state memory technologies.	Aug 1981
Perform initial partitioning studies and make recommendations on requirements and development options (including module/enclosure form factor) for a standard FIR for new Navy aircraft.	Sep 1981
Prepare necessary AVCS support documentation for FIR project.	Continue
Coordinate efforts with Navy organizations and other services (Air Force, Army).	Continue
FY 82	
Prepare FIR request for proposal (RFP) solicitation.	
Coordinate efforts with Navy organizations and other services.	

Publish FIR performance specification.
Prepare necessary AVCS support documentation for FIR project.

6.5 ARCHITECTURE

The primary objective in the selection of an advanced avionics system architecture is the achievement of the required levels of weapon system performance at the lowest possible life cycle cost consistent with the resources that can be allocated to system acquisition.

Avionics of older aircraft were generally non-automated and non-integrated. The collection of platform avionics was heavy, consumed much power, burdened the environmental control system, placed heavy workloads on the aircrew, was prone to error and failure, was difficult to maintain and support, and was outstripped when increased operational requirements arose.

The evolution to more optimum integration, automation, and system flexibility began with aircraft such as the A-7E and A-6E. Further improvements were realized by the F-14 and S-3A. This evolution has been largely enabled by technological progress, including LSI microcircuits, programmable digital processing, and serial digital multiplex communication techniques.

Operational experience with the avionics architecture incorporated in the F-15 aircraft has also demonstrated a measure of the reduction in operation and support costs that can be achieved through state-of-the-art features that include extensive use of bit serial, word serial, multiplexed data transmission between avionic subsystems and the "mission" computer that serves (1) as an executive control center for the avionic system, and (2) as a data processor that generates the majority of the data used for cockpit controls and displays. A network of built-in-test and in-flight monitoring capability is distributed throughout the avionic subsystems and monitored by the mission computer via the multiplexed data bus system. System reconfiguration can automatically occur in the event of malfunctions in primary equipment to retain as much mission capability as possible. The F-18 avionic system also contains these features, with the added capability provided by dual "mission" computers and further employment of digital subsystems that incorporate small and medium general purpose computers for signal processing, dedicated computational tasks, mode control, in-flight checks on subsystem operation, built-in-test for maintenance assistance, and data formatting for the multiplex interface.

Given the reduced reaction time against the anticipated threats and the electromagnetic environment predicated for the 1980s and beyond, it will be mandatory that future avionic systems process and correlate information from many sensors within the weapon system as well as intelligence and other external information. This interdependency will increase the necessity of tradeoff decisions such as functional assignments between on-line and off-line equipments, hardware and software, etc.

In the interval since the inception of the latest generation of fighter avionics, several major technological developments in the field of electronics have taken place that offer new opportunities for meeting the avionic requirements of the next generation aircraft at significant cost

savings in both the acquisition phase and the operation and support phase. The most significant advance is the near-term availability of low cost microprocessors that offer each subsystem manufacturer the opportunity to reduce the number of components required to accomplish the signal processing, control tasks, and logical operations involved in monitoring, data communications via multiplex, and built-in-test. Another significant advance is the rapid development of wide bandwidth signal transmission via fiber optic links. Other technical advances are occurring in specialized areas that are expected to benefit individual subsystems, but lack the broad potential offered by microcomputers and, to a somewhat lesser extent, by fiber optics. The following articles address these architectural areas.

6.5.1 DATA BUS TEST MONITORING, INTERNAL AND EXTERNAL

6.5.1.1 Background

The increasing use of multiplex data bus technology, particularly MIL-STD-1553, has resulted in highly integrated, tightly coupled systems. Such systems, because of their highly interactive nature, require the development of new maintenance philosophies. Failures occurring in one subsystem may result in improper operation of another subsystem or, if proper redundancy is provided, the system may continue to function normally. Built-In-Test (BIT), both at the subsystem and system level, is necessary to provide for fault recognition and fault isolation.

6.5.1.2 Current Status

The use of BIT at the subsystem level has provided a step-function increase in recognizing subsystem failures. These failures can be displayed to an operator via a cockpit display. The operator must log a maintenance request based upon this minimal data. Often, system level BIT is provided to augment the subsystem BIT. Several systems, e.g. F-14A and LAMPS MK III, utilize an extensive off-line system test program. All these systems continue to rely upon the operator to log maintenance requests.

6.5.1.3 Perceived Trends

New systems, such as avionics for the F/A-18, utilize a maintenance data recorder which is connected to the multiplex data bus. While failures are still reported to the operator on cockpit displays, failures are also logged automatically by the maintenance data recorder. Current maintenance data recorders merely log reported failures, however, future versions will be able to analyze multiplex data bus traffic and automatically recognize and log many classes of failures.

As new subsystems with multiplex data bus interfaces enter Fleet use, peculiar test equipment is developed for each subsystem. Each of these peculiar test equipments must contain a multiplex data bus interface.

6.5.1.4 Areas Requiring Further Development

Current - Continued heavy emphasis must be placed upon the development of extensive system/subsystem level BIT. This will become more important as existing systems are updated to include multiplex data bus integration

techniques. Also, further development of maintenance data recorders is necessary. The importance of automatic failure logging with attendant hard copy reporting cannot be overlooked.

Short Term (0 to 5 years) - A requirement exists to develop a comprehensive system/subsystem test set which is compatible with all aircraft utilizing MIL-STD-1553 multiplex data bus technology. This test set must be portable to allow usage on the flight line. The technology used in today's commercially available data bus testers/analyzers can provide the basis for such a test set. Again, extensive use of hard copy failure reporting and failure analysis would facilitate maintenance reporting. This same set of equipment, with additional signal generators and data acquisition equipment, could provide a complete subsystem test set usable at most maintenance levels.

Mid Term (5 to 10 years) - During this time period, fiber optic interconnect systems will be introduced into the Fleet. Some modifications to the interface of the previously developed test sets will be necessary; however, the fiber optic systems will be compatible with the test sets in all other aspects. This time period will also see the evolution of wideband (10-50 megabit per second) multiplex data buses. These data buses will probably use fiber optics as the transmission media, but will use a control protocol considerably different from MIL-STD-1553. The requirements for testing and maintaining such a system must be defined in this time period.

Long Term (10 years plus) - The primary emphasis for this time period must be the development of wideband data bus system and subsystem test sets. The use of interactive voice recognition and speech synthesis may improve the efficiency of these test sets, but the need for hard copy failure logging will not be replaced. Instead, more emphasis will be placed upon automatic reporting of failure information.

6.5.1.5 Development Priorities

Primary emphasis must be placed upon the development of comprehensive system/subsystem level BIT. Further development emphasis should be placed on intelligent maintenance data recorders. To supplement these efforts, a flexible test set must be developed for further fault isolation. Emphasis must be placed on the ability of this test set to isolate problems to the Shop Replaceable Assembly (SRA) level.

6.5.1.6 Summary

The testing and fault isolation of multiplex data bus systems requires the development of capability at several levels. These levels include subsystem BIT, system BIT (both continuous background and off-line), intelligent maintenance data recorders and flexible system/subsystem test sets. Today's requirements center around MIL-STD-1553 data bus systems while future needs will include fiber optic and wideband data buses. A continued emphasis will be placed upon hard copy reporting of failure information and maintenance actions.

6.5.2 WIDEBAND FIBER OPTICS

6.5.2.1 Background

The trend toward a totally integrated avionics suite having increased data transmission requirements will result in data buses or point-to-point links that could require data rates of 100-300 MHZ. Examples of individual systems that could need these large bandwidths are Tactical Information Exchange System (TIES), Advanced Integrated Display System (AIDS), TACAMO, and distributed processing systems using bulk memory transfer techniques.

One of the inherent advantages of fiber optics (FO) technology is the increased bandwidth capability of optical fibers over both twisted-pair wires and conventional coaxial cables. The use of fiber optics in avionics systems requiring a large bandwidth or high data rate is a practical and feasible design approach. This is especially true if the wideband systems have secure transmission or rigid electromagnetic interference (EMI) requirements since FO systems are virtually immune to EMI, and radiate no spurious signals along the transmission path.

There has been little emphasis on wideband FO systems. The extent has been a NAVAIR funded study to determine a possible standard bandwidth for FO data buses, and an investigation of the implementation of a multi-channel fiber optic video data bus for AIDS.

Besides defining applicable systems that could use wideband FO systems, possible architectures need to be considered also. These, depending on system requirements, can include high speed digital point-to-point links, limited access (< 6 ports) data buses (digital and analog), and specialized wideband analog links. All of these potential architectures have viable places in sophisticated avionics suites.

6.5.2.2 Current Status

At present, there are no wideband FO systems undergoing development. The two studies mentioned previously have not transitioned from the study phase into development. A draft specification for a 50 Mbps free access, 16-port fiber optics data bus has been prepared as well as a draft specification for a 10-channel (10 MHz/channel without guard bands), analog fiber optics video data bus. This situation will not change until development funds are identified for these systems.

6.5.2.3 Perceived Trends

A developmental cycle for wideband FO systems will evolve from dedicated point-to-point links to medium speed/bandwidth data buses (50-100 MHz), to high speed/large bandwidth data buses (> 200 MHz). Various versions of a fiber optics video data bus will probably remain as unique applications of the wideband technology. All of these links/buses will necessitate the development of associated transmitter/receiver circuits or modules. These wideband systems will have to use efficient multiplexing techniques, thus methods for optical multiplexing will have to be developed. The data rates of future

avionics systems may dictate the development of higher speed electronic interface logic circuits than now exist. It is expected that all wideband FO systems will use single fiber technology.

6.5.2.4 Areas Requiring Further Development

Current and Short Term (0 to 5 years) - Since no actual development of wideband FO systems has been undertaken in the past and none is planned for fiscal year (FY) 81, the earliest development in this area will not occur until FY 82. At this time, the requirements for the FO system to be fabricated must be determined and the optimal architecture chosen. Optical multiplexing techniques and high speed source and detector circuits must be developed to support these systems implementations. These systems will most likely be the 50-100 MHz variety, and for video data buses. Specifications for these wideband systems and the video data buses must also be developed in this time frame.

Mid Term (5 to 10 years) and Long Term (10 years plus) - The evolution of high speed/large bandwidth fiber optic systems will gradually occur, being driven by the degree of subsystems integration and overall systems complexity. During this period, development should be concerned with systems that require a bandwidth of 200 MHz and above. Due to the speed involved, these systems may be dedicated point-to-point links or very limited access buses. To support these developments, high speed sources and detectors must be developed and integrated with high speed interface circuits.

6.5.2.5 Development Priorities

The development priorities for wideband FO systems will be driven by the individual system that incorporates the technology. However, general priorities can be listed:

* Development of wideband multiplexing techniques (including optical multiplexing techniques),
* Development of general high speed transmitter and receiver circuits/modules,
* Development of specifications for wideband systems, and for a separate FO video data bus,
* Expansion and development of specifications and standards for components, systems, and test methods,
* Development of a family of militarized single fiber connectors (single channel, multi-channel, right/45° angle adapters),
* Development of low-loss optical couplers,
* Continued development of support elements (Navy's funding category 6.2 fiber optics program),
* Across the board development of optical sensors and transducer systems, and

* Development of wideband FO data transfer techniques.

6.5.2.6 Summary

Incorporation of wideband FO systems in military aircraft is several years away. The increased bandwidth capability of FO technology over conventionally wired systems makes the use of fiber optics an attractive design approach for high speed/wide bandwidth avionics systems. The use of fiber optics in such systems should be considered seriously in future avionics systems design.

6.5.3 OPTICAL SENSORS

6.5.3.1 Background

Over the past three years, the Navy has funded research into the feasibility of developing electrically passive, optical transducers for various uses on military aircraft. The general areas in which these transducers can be applied are flight control, propulsion control and data gathering for the on-board air data computer. Specific parameters to be sensed include linear displacement, rotary displacement, temperature, pressure, liquid level, liquid flow rate, compressor blade tip clearance, engine speed and mechanical strain. The investigations undertaken so far have addressed the concepts and techniques to be used for optical transducers and the determination of parameter priority for optical transducer development. Currently, the Navy has an optical linear displacement transducer under development for use on the T-2C aircraft. The Army has developmental efforts for optical transducers which sense linear displacement, rotary displacement and differential pressure. In both cases, these transducers are aimed primarily at flight control applications. There is on-going coordination between the Navy and the Army for optical transducer development. A development program also exists at NASA, Lewis Research Center. This program and the Army's program are being monitored by the Navy to ensure widest sensor development with the funds available to the different agencies. The development of optical sensor and transducer systems is continuing under the Navy's funding category 6.2 program in fiber optics.

6.5.3.2 Current Status

An optical linear displacement transducer system is scheduled to be delivered in December 1980. These systems will be evaluated prior to flight evaluation on the T-2C aircraft; one unit will be attached to the rudder actuator and one attached to the rudder pedal. These two transducers will not replace existing systems, but will be functionally parallel with the existing electromechanical transducers, allowing comparison of their performance with the electromechanical systems. The Army contracts will result in hardware delivered in late 1980 or early 1981.

During FY 80, discussions were held with various Navy Program Offices to determine requirements for the optical transducer systems selected for development with FY 80 funds. The program offices contacted were those of the Full Authority Digital Electronic Controls (FADEC) Program and the Improved Fatigue Life Tracking (IFLT) Program. As a result of these discussions, FY 80 funds are being used to develop feasibility models of an optical

pressure transducer system, a fiber optic strain sensor, and an optical temperature sensor system. The contractual period for these developments will extend into FY 81.

6.5.3.3 Perceived Trends

The number of optical sensors and transducer systems under development is small. For the developments discussed, each transducer system is a single entity; they consist of an optical transducer unit, a signal processing unit and an interconnecting FO link. As the family of optical sensors and transducer systems grow, a bused architecture with a common processing unit for related sensors is needed, but is not being developed currently. The future sensor systems will, in all probability, be grouped according to function, each either using the Standard Airborne Computer AN/AYK-14(V) computer as its processor or having an embedded microprocessor for local processing with a communications channel to the AN/AYK-14(V). Since the data rates for these sensors are not high, MIL-STD-1553 buses or higher speed versions of this bus will be used.

6.5.3.4 Areas Requiring Further Development

Current and Short Term (0 to 5 years) - Coordination between governmental agencies developing optical sensors and transducers should continue, in order to avoid excessive cost, or parallel developments. The optical systems being developed by the Army and NASA can possibly be applied to Navy requirements.

The Army is concentrating on flight control sensors such as linear displacement transducers, rotary displacement transducers, and differential pressure transducer systems that can handle the bulk of the parameter sensing required in flight control. The Army plans to integrate these sensors into a flight control system.

The Navy's program for optical engine control sensors is established, and future development of the sensors is planned. Optical versions of an engine speed sensor, an engine fuel flow rate, and a turbine blade tip clearance sensor must be developed and integrated with the optical pressure and optical temperature sensors to achieve a total engine control package. In addition, an optical blade tip clearance sensor is being developed by NASA that can possibly satisfy the Navy's needs.

The requirements should be determined and development undertaken of a microprocessor-based optical fuel status monitoring system. Optical systems are needed to sense fuel level, fuel flow rate, fuel density, valve position, fuel temperature and fuel pressure. The design approach for these sensors should address a total system basis.

Investigations should start to determine air data information gathering sensor requirements. Sensor developments in other areas should be reviewed to determine if they can be applied in this area.

Mid Term (5 to 10 years) and Long Term (10 years plus) - Optical sensor and transducer technology should have matured to the point that a fly-by-light aircraft design approach can be used.

6.5.3.5 Development Priorities

The following priorities should exist for optical sensor and transducer system development:

* Continued development of the individual sensor and transducer systems for engine control (Navy and NASA) and flight control (Army),
* Development of an optical fuel status monitoring system,
* Development of an integrated bused system for engine control and flight control areas, and
* Development of sensor system for air data information gathering.

6.5.3.6 Summary

The use of a total fly-by-light approach to aircraft design is several years away, but this goal is achieveable. The technology exists to develop reliable optical sensor and transducer systems. The advantages these optical systems offer over conventional transducer systems (EMI immunity, electrically passive sensor, lower weight/volume) will enhance the performance of military aircraft.

6.5.4 FREQUENCY AND TIME STANDARD

6.5.4.1 Background

In recent years, more and more emphasis has been placed on precise frequency and time requirements. This emphasis has come about due to the increase in use of time-dependent navigation systems. The accuracy of the OMEGA system, for instance, is directly related to the accuracy of the time standards involved. In the communications area, precise time and frequency is also becoming a critical element. With a continuing increase in the number of user stations requiring narrow band communications, the use of more precise and stable frequency references is also necessary. Highly stable references are required to prevent unintentional jamming or interference with adjacent bands. Secure communications systems which use pseudo-random codes also require that both sender and receiver have precise time references.

6.5.4.2 Current Status

There are three types of frequency and time standards, each with their own set of advantages/disadvantages, depending upon the application.

* Crystal oscillator-controlled units are the most common and offer advantages of low cost, good short term stability and low power consumption. Their major disadvantage is poor long-term stability.
* Rubidium vapor cell controlled units offer good long-term and short-term stability and faster warmup-time but are more expensive and require more operating power than crystal units.

* Cesium beam controlled units offer excellent long-term stability, but poor short-term stability. They require more operating power than the crystal units, and currently are the most expensive of the three types.

The amount of operating power required for any of these units becomes a critical factor when they are considered for use on an airborne platform. An auxillary power supply must be provided to maintain these units either when aircraft power is removed, or during transit to an uninterruptable power source.

6.5.4.3 Perceived Trends

Due to the reasonably short mission or deployment times of airborne platforms, current trends favor the crystal oscillator-controlled units. Crystal controlled units can provide accuracies of $\pm .5 \times 10^{-10}$ and can be operated in a reduced power mode for 50 hours or more on an internal battery.

Due to the efforts of rubidium vapor cell manufacturers in areas of size and operating power reduction, the rubidium units are receiving more attention. These devices offer considerable advantages in areas where cold starts are acceptable. The rubidium units have a faster warmup time and better stability than crystal oscillators.

6.5.4.4 Areas Requiring Further Development

The Navy, in particular the TACAMO program, has been involved in developing an airborne frequency and time standard system. This system, although developed to meet TACAMO requirements, could also provide the required references for other elements of the Minimum Essential Emergency Communication Network (MEECN). The system currently being developed consists of redundant, portable crystal oscillator standards and an on-time receiver. The time receiver can provide time updates with accuracies of $\pm$ 25 microseconds. These updates are obtained via the Navy Navigational Satellite System. An investigation of this system's applicability to other programs should be performed.

The time receiver maintains time via a crystal oscillator controlled clock. Future units will operate from interchangeable crystal or rubidium controlled oscillators. The rubidium unit would provide the advantage of a faster warmup and a more stable frequency reference which can be used to monitor the drift of the portable crystal units. This system is expected to be granted approval for service use in 1982.

Further developments and improvements should be pursued in the area of crystal oscillators that will provide extremely stable, high quality units in production quantities. Efforts should also be made in the area of atomic standard development, with emphasis on miniaturization and reduction of operating power requirements. The current list of rubidium cell manufacturers is extremely limited. Attempts should be initiated to encourage development of sources of small, military qualified, rubidium controlled oscillators.

6.5.4.5 Development Priorities

The most pressing priority at this time is the development of a reliable frequency and time standard that would provide the stability and accuracy required by the airborne systems in use today and those projected for the near future. Additional efforts should be initiated to further the development of atomic standards that are more suited to airborne applications.

6.5.4.6 Summary

Although considerable advancements have been made in military frequency and time standards and extremely stable systems are available, most of these systems are not suited for airborne applications. The airborne application of frequency and time standards requires units that can be supported on battery power for extended periods of time. This requirement, in conjunction with the other problems associated with airborne applications, increases the design restrictions placed on these standards.

The system currently being developed by the Navy for the TACAMO system will fulfill the requirements of this program for the forseeable future. A continuation of efforts in the development of airborne rubidium, cesium, or other atomic element standards is required to insure that all future requirements for precise frequency and time can be met.

6.5.5 BUILT-IN-TEST/AUTOMATIC TESTING

6.5.5.1 Background

The operational/logistic benefits of various types of automatic testing (AT) techniques for monitoring of end item performance and for rapid, comprehensive detection and isolation of faults in equipment have been recognized for some time. In general, experience has shown that the operational performance of AT has not lived up to these expectations, particularly with respect to field utility and overall cost effectiveness. The principal reason for this less-than-desired performance is failure to recognize and accommodate the need for AT acquisition planning as an integral part of the end item acquisition process. Additionally, the inherent advantages of automatic test equipment (ATE) and, in particular, built-in-test (BIT) for operational readiness, availability and supportability have not been exploited to the degree that current technology would permit.

Failure to include AT concepts during acquisition planning and slow development of BIT are not the only reasons for the generally poor performance AT has shown thus far in the Fleet. Many of the problems AT has experienced have materialized because the fault detection/isolation (testability) technology which forms the basis for ATE design has advanced faster than the disciplines for application of this technology. Also, operational requirements for quicker reaction time, higher performance, and improved accuracy have produced Navy systems designs which have become increasingly complex. This resulting complexity has caused lower Mean-Time-Between-Failures (MTBF), or more failures per system operating hour, and hence created additional demands upon AT capabilities and performance.

6.5.5.2 Current Status

Testing has become a major consideration in the ownership of today's ultra-sophisticated equipments. This is necessitating the exploration of new methods for testing the complex technology being used, of utilizing computers in the quest of viable testing solutions, and of new attempts at developing specification and acquisition documentation that will ensure testability and verification of the results. This exploration is not being limited to one method of test, but rather expanded to all areas of BIT, fault tolerance and AT in general.

This expansion in the field of testing is being aligned in the form of coordinated plans that will direct the efforts of the testing community without duplication of tasks. Plans, such as the Naval Material Command (NMC) plan for automatic testing, are being developed so that the Joint Logistics Committee (JLC) panel and other committees can explore the options and resolve the issues that are retarding the growth of a dynamic AT program.

6.5.5.3 Perceived Trends

The Navy and other military forces are caught in a spiral that demands the earliest introduction of new capabilities and performance that technology can provide. History indicates that introduction of any new technology results in larger, more complex, costlier, and, in some instances, less efficient support systems. As a result, test maintenance and support problems are becoming increasingly more difficult to resolve, and a "gap" between design and test technologies has developed. The continued trend of electronic systems toward increased complexity will significantly impact the test arena. Some of the more significant considerations include:

* A trend toward a test methodology of fault detection in lieu of fault isolation is expected in future systems. This will be brought about by further implementation of non-repairable shop replaceable assemblies utilizing technologies such as whole wafer LSI.

* Complex circuitry, particularly digital, will tax human ability to maintain an orderly and comprehensive accounting of signal flow analysis during circuit design, test generation and repair.

* Due to significantly more complex circuit elements and increased densities, higher confidence levels in terms of successful circuit operation must be achieved prior to hardware mechanization. This, coupled with the two considerations above, established the need to ascertain circuit performance and testability through software simulation programs used as tools for design and test analysis.

* Increased speed of operation and quantity of test stimuli and response patterns in future avionics systems will make automated testing techniques a necessity, not just a means to reduce manpower and cost.

* Short range projections indicate potential system applications of new technologies (e.g., fiber optics) for which supporting test techniques are not fully developed. Systems employing these new technologies could demand test and support techniques which are radical departures from current methods and which may require new and innovative test equipment designs. Research and development efforts to provide a timely and total capability must be addressed.

In analyzing the state of the technologies and trends in avionics systems, one underlying fact becomes clear. The relative importance of the test technology area is increasing rapidly, and a reversal of this trend is not indicated in coming decades.

6.5.5.4 Areas Requiring Further Development

Short Term (0 to 5 years) -

* In 1976 it became apparent that the problems in automatic testing facing the Navy were similar in nature to those of the other Military Services. In recognition of this, the Joint Logistic Commanders (JLC) signed a charter in March 1978 establishing a JLC Panel on Automatic Testing. During 1979, a Joint Service Program Plan was prepared, approved and implemented, thus supplanting a substantial portion of the program, which was formerly limited to just the Navy. The Joint Service Program Plan is grouped into three categories made up of 22 major tasks which, in turn, contain many subtasks. It is anticipated that a majority of these subtasks will be completed within the next five years. The three categories and a few selected major tasks are:

  * MANAGEMENT AND PROGRAM REVIEW

    * Develop policy and procedures for AT specifications, standards and directives, and for evaluating the potential applicability of warranty incentives during the AT acquisition phase.

    * Identify, develop and publish essential documentation requirements to be procured with AT systems.

    * Examine how to best maintain and utilize existing testing corporate memory.

    * Plan and coordinate with industry the AT efforts being supported by the services.

  * ACQUISITION SUPPORT

    * Issue a Joint Service terminology standard (MIL-STD-1309).

    * Develop a set of testability guidelines for Joint Service use.

* Develop a life cycle cost/systems engineering model for optimizing AT support.

* Develop guidelines for selecting, acquiring and validating test program sets.

* Develop a single Joint Service Test Requirements Document in the form of a military standard.

* TESTING TECHNOLOGY

* Develop documentation and tools to facilitate the use and verification of software.

* Develop systems for analog Automatic Test Procedure Generation (ATPG) and digital Automatic Test Generation (ATG).

* Develop testability figures of merit and other tools and techniques to encourage and allow verification of designing for testability.

* Examine emerging technologies and evaluate their impact on AT.

* *The NMC Program Plan for Automatic Testing includes the preceeding items with the additional category of "ATE Acquisitions and Improvements". This additional category combines the individual Systems Commands plans for the acquisition and improvements of automatic testing hardware intended for multiple weapon sysetms application and its associated software. Subtasks descriptions, milestones and estimated funding requirements are contained in the JLC and the NMC program plans. The plans should be implemented and updated as necessary to enhance the AT and BIT capabilities of the services involved.*

Mid Term (5 to 10 years) -

* Update JLC and NMC Program Plan by expanding current tasks and/or assign tasks so as to:

* Strengthen ATE managment structure,

* Optimize use of ATE in the Navy,

* Improve off-line test capability,

* Improve in-system test capability (including BIT techniques),

* Develop preferred monitoring circuits, and

* Establish standard testability figures of merit.

Long Term (10 years plus) -

* Update JLC and NMC Program Plan by adding tasks that enable AT to maintain pace with advancing technology by developing:

  * Test methods commensurate with high component densities predicted for use in advanced packaging concepts,

  * Fault tolerant computing systems, and

  * Computer aided design techniques capable of verifying testability of system designs.

6.5.6 REDUNDANCY WITHIN SUBSYSTEMS AND SYSTEMS

6.5.6.1 Background

The mission success of modern Navy aircraft depends upon the avionics complements' continued operation despite subsystem and component losses to battle damage and/or insufficient maintenance. Battle damage survivability is greatly enhanced by the use of distributed protective redundancy. The present lack of Fleet maintenance capability for new, complex technology has made self diagnosing and repairing systems a necessity if operational readiness is to be maintained. At present, the only known methods for providing fault-tolerance capability is through the use of excess (redundant) hardware. That is, the system contains more hardware than is required to perform its mission, *even if no components fail*.

There are many forms in which redundancy can be employed to provide fault-tolerance. Some definitions are:

* Explicit redundancy - System/subsystem components are physically replicated and interconnected such that a failure can be detected and the faulty component replaced by a failure free unit. Dual redundancy, triple redundancy with voting, and quad redundancy are terms that refer to various implementations of explicit redundancy.

* Implicit redundancy - The system/subsystem consists of a set of resources interconnected in a very general manner. More resources are available than required for the mission. Available resources are dynamically assigned to tasks as required, using a de-centralized control scheme. Failure of a unit results in its automatic removal from the interconnection facility. Thus no unusual action is required by the software or control mechanism. Implicit redundancy schemes have been demonstrated for Single Instruction Multiple Data Stream (SIMD) architectures.

* Functional redundancy - System resources are allocated to operational functions at design time. Various classes of faults are defined and a system response to each fault class is determined. Hardware and software resources are provided to execute these pre-defined responses. Fault detection and isolation is used to identify the fault class and initiate the response.

* Critical component redundancy - Selected components of a system/subsystem are replicated and interconnected such that failure in a component will result in its replacement. This concept can result in effective dual redundancy at lower cost and weight penalties and has been demonstrated in ultra-reliable satellite and spaceborne equipment.

6.5.6.2 Current Status

Today's technology has given us components whose lifetimes are in the order of one failure per 10^{10} hours of operation. Avionics equipments are, however, extremely complex, consisting of thousands of electronic elements. The state-of-the-art has advanced to the point where the few failures that occur are random. This has effectively nullified the approach of scheduled replacement and testing during maintenance. Research results and design experience over the last decade have shown that the systematic introduction of protective redundancy to provide fault-tolerance can be accomplished, both at the microcircuit level (on-chip redundancy), and at higher component and subsystem levels.

Historically, a significant increase in the number of gates employed in a design (as in redundancy) has translated directly into a similar increase in system cost. Very Large Scale Integrated Circuit (VLSI) technology revises these economic guidelines by permitting the addition of on-chip circuitry at very low cost. Presently, the potential exists of increasing the fault-tolerance of systems by adding circuitry while holding both performance and cost essentially unchanged. It has been estimated that the penalty for fault-tolerant design implemented in VLSI can be as low as a 5.5% increase in chip count.

System complexity has grown dynamically as a result of increased demands for higher levels of system performance and capability. This complexity has been growing at a faster rate than advances in component reliability. This increased complexity results in lower reliability, unless protective redundancy is applied.

Emphasis upon transient as well as permanent fault survival for avionics equipment is a crucial issue. A system should not produce erroneous results even in the presence of faults.

The advent of physically small, inexpensive computational hardware has made the concept of system and subsystem level fault-tolerance feasible. Investigations of fault-tolerant hardware and software design approaches are being pursued within specific project efforts, primarily satellite and space equipment. Fault-tolerance has always been, and continues to be, a major problem in the design of flight control systems, especially the new fly-by-wire systems. Fault-tolerance work in avionics is specifically directed towards particular platforms. Generic methodologies and guidelines are in early stages and have not yet been applied to Naval avionics. This lack of generality reduces the capability of present fault-tolerant systems when their hardware complement is modified or extended.

Much work remains to be done in the creation of models which accurately reflect the real complexity of avionics software, hardware, and operation.

6.5.6.3 Perceived Trends

In the avionics area, functional redundancy within heterogeneous multi-computer systems is the present trend, and will probably continue for some time. This is not an optimum solution, however, and parallel work on implicitly redundant systems will continue and expand, especially in the signal processing area.

Complimentary Metal Oxide on Silicon (CMOS) technologies are likely candidates for future military application due to their low power, high density and radiation hard characteristics. Potential densities for the late 1980's are 100,000 gates per chip.

Military application of VLSI technology will lag commercial development by several years.

A trend towards modular design of avionics equipment is evident. Studies and system work have established maintenance, reliability, and enhanceability incentives for modular design.

6.5.6.4 Areas Requiring Further Development

Current -

* Fault-tolerant design methodologies.

* Identification of fault classes.

* Extension of fault-tolerant features to effect automatic maintenance.

* Development of models which reflect the real complexity of avionics systems.

Short Term (0 to 5 years) -

* While added measures of fault-tolerance may be achieved through software techniques, software transparency must be maintained. Methods must be developed that do not require modification of this application software for execution in processors whose only difference is level of fault-tolerance.

* The number of possible faults in a large distributed system is, for all practical purposes, infinite. A method must be developed for specifying fault-tolerance in an understandable and measurable format.

* Standard interface protocols and high speed processor-to-processor buses must be developed to allow rapid reconfiguration and efficient distribution of data.

* Efficient reconfiguration strategies and architectures amenable to their implementation must be developed. Testability and reconfigurability must be incorporated in systems in the design phase.

* Development of design methodologies for fault-tolerant systems.

* Development of computer aids for fault-tolerant design for LSI circuits.

* Assessment of life-cycle cost drivers.

* Integration of fault-tolerance technology with modular avionics.

Mid Term (5 to 10 years) -

* Evaluation tools and methods for measuring fault-tolerance must be produced.

* Fault-tolerance VHSIC functions must be produced to reduce size and weight penalties presently incurred.

* Architectures using implicit redundancy should be developed, since they are inherently fault-tolerant.

* Major avionics systems utilizing a high degree of fault-tolerances must be developed.

* VHSIC devices that accommodate fault-tolerance, without sacrificing system performance, should be developed.

Long Term (10 years plus) -

* Reliable, self repairing avionics systems that utilize VHSIC technology and standard interface protocols must be demonstrated.

* Unified maintenance, instrumentation and design methodologies for entire avionics complements must be generated.

6.5.6.5 Development Priorities

General self-checking combinational logic design procedures must be developed. Some major building blocks have been developed, but many more require development.

Significant problems exist in using some conventional fault-tolerant techniques for VLSI. Modified approaches must be investigated wherein fault detection responsibility is placed within the chips to be tested.

Fault-tolerant VLSI cell libraries (equivalent in function to existing cells used in integrated circuit design) require development. The production of a fault-tolerant chip could then be easily derived from any fault-intolerant chip design. Techniques applicable to this concept include:

internal redundancy using complementary logic, error detection/correction codes, redundancy and inter-chip network checkers, and self checking error checkers. Conceptual simplicity and ease of use must be accomplished for wide spread use of fault-tolerant design.

With the increasing use of micro-code for system design, error correcting codes on the micro-store contents becomes important. Error free performance of the micro-store is much more important than main memory reliability.

Fault-tolerance requirements and design guidelines must be established. Standardized multi-level interface protocols must be defined and implemented in high-speed buses (probably fiber optic), and reconfiguration strategies for avionics systems must be defined and demonstrated.

6.5.6.6 Summary

Physically small and inexpensive computational hardware provides an attractive mechanism for addressing the Navy's need for fault-tolerant systems. Fault-tolerance concepts are presently being developed for specific applications, but no generalized methodologies or guidelines are available. Specification and evaluation of fault-tolerance is difficult. Implementation of fault-tolerance in Naval avionics systems requires the definition and imposition of standardized, multi-level interface protocols, and the development of high-speed, processor-to-processor buses. The VHSIC program allows the implementation of fault-tolerance functions to reduce the size and weight penalty incurred by using redundant hardware.

6.5.7 GENERAL ARCHITECTURAL CONSIDERATIONS

6.5.7.1 Background

The technology explosion offers the avionics world unprecendented opportunities in size and weight reduction, improved reliability and maintainability, and mission flexibility. These improvements in technology are required to achieve the multi-mission capability planned for many aircraft in the 1980s and 1990s. The effective utilization of these advanced technologies, especially digital integrated circuits, will require that the nature of the avionic architectures change drastically. With the advent of low cost, small, and functionally powerful microcomputers, distributed processing applications will increase at a rapid pace. This will result in subsystems that interact with each other to a much greater extent than now occurs. The disciplines required for the acquisition (including specification, design, test, integration, documentation, and configuration management) of such advanced avionics must be developed by the NAVAIR Acquisition Managers and their respective support activities.

NAVAIR has recognized the potential problems inherent in the acquisition of the types of avionics required over the next two decades and has taken a number of actions to become prepared. One of these actions is the establishment of the function of Avionics Architect in NAVAIR with support for this effort by NAC and NADC. This function provides technical support to NAVAIR Program Managers (PMAs) and Acquisition Managers (AMs) in the area of

avionics architecture. In addition, the function will provide specifications for hardware/software/firmware interfaces for Naval avionics systems and will develop and apply the complex disciplines required for system design, test, and configuration management. The function will provide inputs to the NAVAIR Avionics Master Plan (NAMP) particularly in the areas of electrical interfaces, data bus plans, and recommendation of potential GFE candidates. It will also provide inputs to Research and Technology Administrators in AIR-03.

The likelihood of successfully incorporating new technologies and architectural concepts into developmental platform programs can be enhanced if the payoffs are demonstrated starting in the concept validation phase and continually evaluated during the useable life of the equipment. Recognizing this potential, NAVAIR has initiated a program to develop facilities for the orderly transition of technology to Fleet use and for the continued support of these equipments throughout their life cycle. These facilities consist of:

* The BASIC Avionics System Integration Concept (BASIC) Laboratory at NADC.

* The proposed Flight Test Bed Aircraft (FTBA) program.

* The Digital Avionic Systems Laboratory (DASL) at NAC.

These facilities will be essential in the development of methods to deal with the wide spread future need to emulate, simulate, stimulate, test and evaluate digital data bus structured systems, subsystems and components during feasibility study phases, design, development, test, diagnostic, manufacturing, repair and life cycle support.

Both the BASIC and DASL facilities provide advanced system processing architecture configurations for the integration of new technologies. The BASIC Laboratory provides the capability for evaluation of different sensor and processing architectures, system integration technologies, technology alternatives, platform issues, and candidate system performance for developmental (6.2, 6.3) equipments in a conceptual system environment. The DASL performs similar functions for equipments in Engineering Development (6.4) and production (6.6) in addition to providing support during the life of the equipments. The laboratories are structured around the MIL-STD-1553A/B multiplex data bus standard with multiple AN/AYK-14 Standard Airborne Computers and other programmable resources in distributed configurations. These configurations provide the flexibility required to evaluate avionics alternatives

through either the incorporation of advanced technologies or existing hardware and through the use of subsystem simulation. By taking advantage of the capabilities of these laboratories to simulate a wide range of avionic system configurations, the integration of advanced subsystem technologies into existing or projected platform systems can be verified experimentally. This verification feature will be used to examine the impact of proposed avionic changes to new aircraft or aircraft CILOP programs as well as providing production and In-Service Engineering support.

The FTBA will allow for systematic implementation of equipment and subsystems to validate performance and demonstrate operational utility in a real-world test environment. The avionics of interest will not be limited to core avionics, but will extend to mission avionics as well. Flight validation, a far more costly operation than laboratory integration of systems and technology, will be conducted for those selected advanced technologies and subsystems warranted by successful BASIC or DASL Laboratory demonstration.

6.5.7.2 Current Status

The Avionics Architect function in NAVAIR has recently been established, and efforts are in progress to define the total role this function would assume in overall NAVAIR acquisition process. The following are some of the more important responsibilities of the Avionics Architect:

* Establish NAVAIR avionics architecture policy for electrical interfaces, excluding power. These interfaces will include the multiplexed serial data bus (e.g., MIL-STD-1553), wideband video bus, and other buses and dedicated signal lines required to communicate data between subsystems. The architecture policies established by the Avionics Architect will be equally applicable to Government Furnished Equipment (GFE) and Contractor Furnished Equipment (CFE).

* Recommend candidates for common GFE (and CFE) avionic development, based on the projected needs of existing and future avionic systems. The Avionics Architect and his staff will participate actively in the generation and updating of the NAMP and will develop advanced equipment requirements guidelines.

* Assist the AM in development of the guidelines and requirements for inclusion in equipment specifications that will ensure the compatibility of the subsystem with the avionic system archi-

tectures. The guidelines and requirements might include, but not be limited to, the following topics: multiplatform considerations, standardization concepts/policies, subsystem partitioning/interactions, maintenance and logistic concepts, interfaces (electrical/thermal/mechanical/environmental), built-in-test (BIT) concepts, reliability requirements, safety considerations, human factors, life cycle cost (LCC) considerations, data requirements, and test and evaluation concepts.

* Assist the AM in evaluating the performance and external interfaces of common GFE test articles. This evaluation may be performed on a hot bench designed to simulate or duplicate the avionic system interfaces and interactions with the common GFE test articles (e.g. BASIC or DASL). Also, this evaluation may be used to assure that the bus-structured system can be effectively tested and supported by maintenance activities.

* Assist the AM in test and evaluation planning, acquisition strategy development, contractor proposal evaluation, and other project planning and/or evaluation that is architecture-related.

* Assist the AM in the definition and design of the hardware and software support facilities to be used by the Cognizant Field Activity (CFA).

* Provide guidelines and goals to NAVAIR-03 Technology Administrators that will ensure that avionic system architecture considerations are included in category 6.2/6.3 technology development projects.

* Work with the Technology Managers to ensure awareness of new and emerging technologies. The management of application of new technology to developmental systems is a critical task which the Avionics Architect must coordinate with the TTCs.

* Conduct studies on a continual basis of advanced avionic architecture concepts and implementation techniques. Interfaces must be maintained with Navy Centers and Laboratories and industry to ensure awareness of new architecture concepts.

* Maintain the DASL and BASIC Laboratories to simulate or duplicate avionic system architectures and subsystem/system interfaces and interactions.

Current trends in avionics systems are moving away from the traditional stand-alone, vertically-integrated "black box" approach to horizontally-integrated subsystems. Advances in digital technology have driven systems design toward the sharing of resources, particularly in the processing, control and display areas. It becomes increasingly important to consider the impact of new developments on postulated system configurations early in the development/acquisition cycle, and simulate these approaches in a laboratory configuration.

The configurations that are evolving in the BASIC Laboratory and being supported in the DASL Laboratory are applicable to a wide range of missions and platforms. These configurations are currently composed of the latest technologies including:

* Multiplex data distribution integration,

* Integrated, programmable, multifunction displays and controls,

* Distributed processors,

* Microcomputer signal and data processing,

* Integrated communication, navigation, and identification,

* Fiber optic data buses, and

* Stores management processors.

The FTBA bridges the gap between laboratory evaluation (BASIC) and Advanced Platform or CILOP configurations. The DASL follows these configurations providing production and life cycle support. The FTBA will provide flight evaluation of these systems configurations that have been proven worthy of advanced platform implementation through laboratory evaluation. The FTBA is currently in the proposal stage to study such topics as:

* Detailed descriptions of avionics architecture available,

* Acquisition plan for hardware and software,

* Programmatic issues such as identifying immediate and long term R&D/CILOP/SLEP programs that would benefit from FTBA operations, and

* Detailed milestones and costs.

The initial phase consists of the installation (on the flight test bed aircraft) of an AN/AYK-14 Standard Airborne Computer, a MIL-STD-1553 data bus, several microprocessors, a multipurpose programmable display, and a data retrieval system. These equipments would provide the aircraft with a basic capability to support many of the new technologies with minimum capital investment. This capability would be separate from the aircraft's flight essential core avionics.

A second avionics implementation phase would be undertaken after the avionics of the initial phase had been installed and thoroughly evaluated. This phase would provide specific core software capabilities, including a full capability executive and bus controller. In addition, interfaces would be provided for the core avionics equipment (i.e., aircraft navigation and communication).

Subsequent phases of the test-bed avionics development would include enhanced support-software, antenna systems, a more sophisticated electrical distribution system, advanced displays, a flexible avionics architecture, and

any other avionics that are necessary to support the new technologies and CILOP/SLEP programs.

6.5.7.3 Perceived Trends

The interdependency among subsystems will continue to be a major thrust of systems development. This trend will most notably be observed in the areas of embedded microprocessor applications, the sharing of processor resources, and the implementation of shared controls and displays. The availability and use of these shared resources will result in less emphasis being given to centralized computer architectures and greater emphasis being placed on federated or distributed processing configurations.

The use of these advanced configurations will enhance the ability of designers to provide systems that have increased reliability through redundancy and fault-tolerant system designs. Greater emphasis will also be given to self-test and automated fault reporting utilizing the capability of embedded microprocessors in "smart" subsystems.

This subsystem inter-dependency creates severe problems in total system test, configuration management, and documentation. The Avionics Architect and associated support personnel must address these problems and generate guidelines and policies to ensure that these problems do not recur. The BASIC Laboratory will be invaluable in the evaluation/verification of these techniques. Similarly, the DASL Laboratory will provide a much needed function in the application of these guidelines and policies during the production and life cycle phases of those systems selected for advanced platform usage.

Standardization efforts are continuing in the areas of data buses and interface definitions for the various aircraft subsystem interfaces. These standards are the results of cooperative efforts of both the military and industry. Beyond the serial, time-division multiplex, 1 Mbps MIL-STD-1553B data bus, definition efforts are in process for wideband, serial, data buses (including fiber optics) and for high speed, parallel processor-to-processor data buses. Standard aircraft interface definitions are being discussed [like the aircraft-to-stores (smart weapons) standard (e.g. MIL-STD-1760)].

Efforts should continue in definition of standard aircraft interfaces (e.g. MIL-STD-1760) and on the cooperative generation of military standards for new types of data buses (e.g. wideband, serial bus).

The Avionics Architect function should be utilized to provide advanced architecture acquisition guidance to the PMAs and AMs for all NAVAIR programs. The support of the NAVAIR Avionics Architect function by the designated field activities should be expanded and strengthened to address problems associated with increasingly costly and complex avionic subsystems.

The perceived enhancement in the aircraft avionics will not be achieved without cost. Appreciable effort must be given to the development of broadband busing architectures for processing handoff and to the development of executive control techniques for distributed processing architectures.

In addition, greater emphasis must be given to the inter-dependency of avionic subsystems. These configurations must be developed early in the development cycle to enhance the subsystem interplay. In general, the trend is toward the transitioning of a total system through the development cycle, in lieu of the traditional subsystem or "black box" approach.

In keeping with these perceived trends, the capability of the DASL and BASIC Laboratories to incorporate selected state-of-the-art advances in avionics technology will be continually upgraded. Current trends in the laboratories include an evolution to high-speed (greater than 50 megabits per second) and wide bandwidth systems. The laboratories are also being used to explore the applicability to the avionics interface problem of distributed processing schemes, fiber optic data buses, the embedding of microprocessor resources in sensor avionics, and voice interactive technology. They are being used to place increasing emphasis on software solutions to traditionally hardware problems (e.g., multi-sensor correlation algorithms).

6.5.7.4 Areas Requiring Further Development

Current - Continued emphasis must be given to the application of MIL-STD-1553 multiplexing and application of the Navy AN/AYK-14(V) standard airborne computer. Use of the multiplex busing structure will help alleviate current retrofit difficulties, simplify the incorporation of new technologies and aid the incorporation of system diagnostics and self test. Similarly, the application of the AN/AYK-14(V) where practical will help alleviate the current proliferation of non-standard computers and non-interchangeable system software.

Short Term (0 to 5 years) - Developmental efforts for multiplex bus control techniques are required. The ability to apply dual controllers in a control and monitoring mode to assure redundancy and fault control has not been fully exploited. Additional efforts are required to determine effective methods of fault-detection, fault-recovery, and bus and controller switching.

Emphasis, in the short term, must also be given to the system applications of higher order languages, particularly ADA.

Continued effort must be provided in integrated control and display functional groupings of subsystems.

In addition to the previously mentioned Avionics Architect functions, a set of general avionics architecture guidelines and instructions should be prepared to identify standard interfaces, standard avionic subsystem recommendations, Built-in-Test (BIT) guidance, interoperability considerations and information on improving mission reliability and degraded mode operability.

The capabilities and utilization of the BASIC and DASL laboratories must be expanded significantly to develop the tools and techniques necessary to introduce high technology and advanced architecture into Navy avionics systems in a timely manner and to provide continued support during the usable life of these production equipments.

The FTBA concept study should be completed as well as Phase I and Phase II of equipment installation on the FTBA. Subsequent phases of the FTBA will evolve as a function of specific flight test requirements. Specific advanced avionic system investigations will be transitioned during this period from the BASIC facility into the testbed aircraft. These systems considered worthy of production, as a result of the preceding laboratory and flight test evaluation, will transition to the DASL for production and life cycle support.

Mid Term (5 to 10 years) - Developmental effort for high speed busing applications is required in the mid-term. Particular emphasis is required in fiber optics technology. Increased usage of fiber optic multiplex buses during this period requires the development of new network topologies due to the interconnection constraints imposed by fiber optic coupling technology. Other broadband media should also be considered.

The impact of broadband busing applications on avionic systems must be determined. The application of broadband busing technology and embedded processing resources will drive systems to the application of truly distributed processing architectures. To achieve these architectures, development of distributed executives for control of these advanced distributed system architectures will be required.

Emphasis must also be given to the development of decision aids and voice interactive technology in the mid-term. As complex systems develop, appreciable efforts must be given to off-loading the work of already overburdened aircrew.

The Avionics Architect function should be continually evaluated to determine if the advent of new technology, architectures and design methodology indicate an expansion or change in the role of this function. The avionics architecture guidelines should continue to be expanded and updated.

Long Term (10 years plus) -

Developmental efforts will be required to apply VHSIC and mini/microprocessors to aircraft systems. The next generation of processors will be appreciably smaller and contain much more memory than existing avionics computers. The application of these resources to avionics will necessitate appreciable systems development, integration, and evaluation effort. The evolution of VHSIC technology will result in a family of macro-functions capable of application across a broad range of avionics functions. Assessment of these applications is mandatory.

With the development of enhanced processing capability, a trend toward the application of artificial intelligence to avionics system development is envisioned. Efforts to assess the application of artificial intelligence to avionics systems will be necessary.

The interface standards that are being developed should also be coordinated with NATO organizations. Potentially, there could be common subsystems which would work in different countries' aircraft. This is especially important for avionics associated with certain air-launched weapons which are to be used by several NATO countries.

6.5.7.5 Development Priorities

Continued emphasis must be given to the implementation of developmental areas mentioned in the previous section. The application of these technologies must evolve in a systematic fashion.

Critical to the successful management of technology and architecture insertions into the system acquisition process is the establishment of the NAVAIR Avionics Architect function, and adequate support for this function. This management function can be greatly assisted by the generation and utilization of the proposed Avionics Architecture Guidelines.

The BASIC and DASL laboratory implementation of the systems' technologies described previously will be mandatory to assess the impact of advanced configurations on avionics development and to assess the impact of selected technologies on production systems. These areas stress the trend away from stand-alone subsystem development toward the transition of total avionic system developments. A time-phased approach (in the order presented) to the implementation is envisioned:

* Multiple bus controller technology,
* Higher order languages (ADA),
* High-speed busing technology,
* Integrated avionic system multi-function control and display technologies,
* Distributed executives,
* Voice interactive systems control,
* Decision aids,
* Advanced processing resources,
* Advanced systems architectures, and
* Artificial intelligence.

As these technologies evolve, they must be incorporated in a laboratory systems environment to assess avionics subsystems impact. The FTBA must then be used to provide continuing assessment of these systems in a flight environment.

Several aircraft configurations (LAMPS and F-18) currently exist that utilize MIL-STD-1553A configurations and the AN/AYK-14 avionics computer. The DASL Laboratory will initially support these configurations, particularly in the areas of production and life cycle support, and will evolve to incorporate additional configurations as the need arises.

6.5.7.6 Summary

The Avionics Architect function provides NAVAIR with the tools necessary to effectively manage advanced avionics acquisition and configuration control efforts. The DASL and BASIC Laboratories and the proposed FTBA provide for the orderly transition of avionics technology. The laboratory facilities include advanced system processing architectures for integrating and evaluating emerging technologies. The FTBA will provide performance validation in a real-world environment. A major trend in avionics development is greater inter-dependency among subsystems (i.e. horizontal integration, shared multifunction displays and controls, embedded microprocessors, distributed data processing).

Inter-dependency will also require the development of broadband busing architectures and the simultaneous development of the various subsystems.

The BASIC and DASL laboratories and the FTBA will incorporate emerging technologies to assess their impact on avionic systems. Through this continuing evaluation an assessment will be made to determine their suitability for aircraft use. Additional benefits achieved from this process include:

* Risk assessment,
* Architectural, processing, and technology alternatives,
* Flight environment evaluation,
* Integrated laboratory and flight test approach to systems development,
* Enhanced technology transition,
* Production support, and
* Life cycle support.

Concurrent with the continuing assessment of technology and the support of existing or new systems, the BASIC and DASL facilities will evolve through:

* Continued development of core and mission avionics evaluation facilities,
* Growth of centralized data bases.

6.6 AVIONICS STANDARDIZATION PROGRAMS

In numerous cases, avionics systems/subsystems have been developed to satisfy a specific requirement for a specific platform, resulting in numerous systems of similar characteristics, but each tailored to satisfy a unique airframe requirement. In other words, avionics developments have not

been approached with a wide-angle vision of all potential Navy and other military service platforms to establish an optimum level of hardware and software commonality within these weapons systems.

The high cost of maintaining current avionic systems is, in part, due to this multiplicity of equipments performing similar functions. In addition, the escalating inflation factor combined with a relatively constant dollar defense budget has "shrunk" the buying power available for use in the development of new avionic systems. In light of this dichotomy, with no reversal of the trends in the foreseeable future, steps must be taken to achieve a higher degree of platform commonality in future avionics.

If we examine the stimuli for non-commonality of avionics between platforms, we find that newly specified weapon systems "can't use" existing items because of either functional limitations, electrical interface incompatibility, installation incompatibility, inadequate or undefined reliability and maintainability provisions, or because the standard item "belongs" to another service branch. However, as formidable as achieving commonality might appear in light of these dilemmas, the application of a coordinated systems engineering approach, coupled with advanced technologies, afford the opportunity for the Naval Air Systems Command to achieve significantly increased platform commonality of avionic systems/subsystems.

This coordinated systems engineering approach must include the following factors:

* Identification and analysis of the functional requirements of each potential platform, and the establishment of consolidated, integrated multiplatform requirements.

* Establishment of standardized electrical, mechanical, and thermal interfaces and installation requirements.

* Establishment of realistic reliability and maintainability requirements.

* Establishement of weight and size requirements based on requirements of the potential platforms.

Several ongoing NAVAIR programs are designed to address these factors. These programs have found that a digital mechanization of avionics subsystems lends itself to partitioning into groups of identifiable functional elements. The size of these functional elements may be large or small, depending on the amount of functional sub-dividing required by the system specifications. By comparing functional elements resulting from the partitioning of a variety of digitally-mechanized subsystems, a core set of functional circuits which have high commonality across these subsystems can be identified. Hence, functional standardization at a level below the subsystem is feasible and practical.

The complementary effects of these programs will allow the Navy to:

* partition electronic functions in a manner that will achieve high hardware commonality within many equipment applications,

* ease the logistics support burden on the congested supply system by extensive intersystem commonality of a limited number of module types,

* reduce life cycle costs as a result of all the above,

* minimize the technology dependence by documenting modules with functional specifications, allowing a measure of "technology transparency", and

* achieve high reliability through stringent quality assurance and design requirements focused upon these fewer module types.

6.6.1 MODULAR AVIONICS PACKAGING

6.6.1.1 Background

Historically, avionics have been procured as discrete "black boxes," each dedicated to a specific avionics function, and with little control over details of internal construction. This approach to avionics procurement has resulted in a proliferation of unique system designs, hardware implementations, and unique logistic support considerations. Standardization of, and commonality in, the avionics equipment has typically been applied only at the subsystem level. Future avionics need not only to be more reliable and maintainable; but must also be lighter weight, more supportable, and must achieve these characteristics at lower life cycle costs. These seemingly contradictory objectives require innovative and revolutionary approaches to the packaging of future avionics, in both the advanced higher performance aircraft as well as in major retrofit applications such as Conversion in Lieu of Procurement (CILOP) programs.

Although the unique "black box" approach may appear to provide the best cost, performance, reliability, and timely availability of new avionics due to the extremely competitive environment provided by multiple suppliers, each exploring different approaches, frequently the reverse is actually true. The life cycle cost of equipment so acquired is higher due to unique design costs, additional spare parts cost, unique ground support equipment and maintenance manuals, training costs, etc. The performance has often been degraded due to environmentally induced failures caused by inadequate packaging. The reliability may be lower if insufficient emphasis is placed on thermal performance. The system may not be timely in its availability because designers "re-invented the wheel". For these reasons, the Naval Air Systems Command initiated a program known as Modular Avionics Packaging (MAP) to attack the problem areas.

6.6.1.2 Current Status

The objectives of the MAP program are to identify, develop, and implement packaging concepts that will satisfy the stringent high density, light weight, high reliability, and high maintainability requirements of NAVAIR avionic equipment/systems. Primary packaging approaches under consideration are the integrated rack (IR), standard enclosurue (SE), and use of standard avionics modules (SAM). The IR combines groups of SAM into subsystems or multiple subsystems and provides all required interconnections,

mechanical and environment protection, and cooling. By standardizing the module interfaces, power supplies, and cooling techniques, the IR will provide a more reliable, maintainable lighter weight avionics package. For applications where an IR cannot be used, a SE is being considered. The SE will also utilize the SAM module. Thus, the primary outputs of this effort will be the development of an integrated rack, a standard enclosure, and ultimately standard modules, all of which are designed specifically to satisfy the unique requirements of avionics.

Numerous studies have been performed to develop the NAVAIR IR concept. Currently, a contract has been awarded to an airframe contractor to produce a developmental specification for the IR. The contractor is also in process of developing a proposal to implement an IR packaged system in the A-6 aircraft.

A contract has been awarded for an SE development study. This study will develop the concepts required to allow use of "building block" standardized enclosure hardware in future Navy avionics systems. The study will also address improved cooling of SAM through the use of "flow through" module configurations. The enclosures will be based on the Austin Trumbell Radio (ATR) box size used by the commercial airline industry, and currently used (with some perturbations) by many avioncis producers.

Two versions of SAM have been identified, and are in the process of being developed. These versions are the Format B, which is currently a standard module form factor of the Navy's Standard Electronic Modules (SEM) Program, and a compatible new module form factor known as the 1/2 ATR, which is based on the 1/2 ATR enclosure size. Hardware elements for the Format B are currently being multiple sourced in industry. An intensive program to design, develop, test and multiple source the 1/2 ATR hardware is in process. Commonality of hardware elements between the Format B and the 1/2 ATR module (such as connectors, keying bushings, keying pins, etc) will allow acceleration of the development process and result in further reduction of life cycle costs.

6.6.1.3 Perceived Trends

Previous engineering design controls and policies in areas of configuration control, standardization, logistics, etc., have been keyed to packaging approaches which were based on the low complexity factors of discrete semiconductor and small scale IC devices. Increased focus is not being placed on higher level, technology transparent packaging techniques which are required to cope effectively with the volatile nature of technology advancements and obsolescence. The effectiveness of these policies can be evaluated by measuring the present state of technology utilization in contemporary avionics and noting that reliability, maintainability, availability, and logistics support problems, and escalating costs are seriously degrading the readiness factor of defense avionic systems. The proper application of advanced packaging techniques could significantly reduce the level of these deficiencies in future systems.

The following problems are predicted for Navy equipments in the future, if the past policies and approaches to the procurement and support of avionics systems are continued:

* High redesign and requalification costs of modules and subsystems would be experienced.

* Production and logistics delays would result.

* Many products would be sole source and subject to instant unavailability.

* Long redesign/requalification cycles would occur for equipments mechanized in rapidly obsoleted technologies, with a proportional reduction in system availability or capability.

* Avionics equipments would be mechanized in outdated circuit architectures.

* The high cost of ownership of avionics equipment would continue to increase.

Numerous areas in the thermal and packaging fields have the potential for improved thermal control, packaging efficiency, and/or improved functional performance. The NAVAIR MAP program is carefully selecting and developing those areas specifically required for optimum SAM, IR, and SE concepts. New concepts in thermal control, power distribution and backplane technologies, and improved circuit board technologies are of primary importance.

6.6.1.4 Areas Requiring Further Development

Short Term (0 to 5 years) -

* Develop and multiple source module hardware in both SAM form factors. (ISEM and 1/2 ATR)

* Investigate and develop improved power and signal distribution techniques.

* Develop SE hardware for individual system use.

* Develop IR concepts further, and evaluate their use in new aircraft or major force modernization efforts.

* Develop maintenance concepts which support the use of IRs.

* Provide strong Navy policy and guidelines in the use of SAM, SE, and IR hardware for new avionics developments.

* Develop demonstration systems in the SE and the IR.

Mid Term (5 to 10 years) -

* Develop additional SAM elements required to accommodate VHSIC devices, both at the module level and the next level of assembly.

* Develop application guidelines for SE and IR implementation.

* Provide on-going standardization support.

* Develop and multiple source additional selected standard functional entities.

* Implement hardware standardization in all applicable avionics developments.

Long Term (10 years plus) -

* Develop the next generation of SAM form factors and next level of assembly hardware supportive of new development electronic components.

* Develop and source additional selected standard functional entities.

* Provide ongoing standardization support.

6.6.1.5 Development Priorities

* Develop standard module hardware elements.

* Develop SE and IR hardware elements.

* Develop demonstration systems in SAM and either SE or IR (or both) configurations.

* Mandate use of these approaches for new avionics developments.

6.6.1.6 Ongoing Programs

MAP Development Efforts

The following milestone information is provided to give an indication of the availability of hardware elements within the MAP program. Availability of elements is dependent on funding allocations, but the milestones shown reflect current plans.

MILESTONES

FY 81	
Format B Hardware Availability	Current
1/2 ATR Hardware Development	Apr 81
Preliminary IR Specification Available	Apr 81
SE Study Complete	Jun 81
IR and SE Concepts Available for System Development	Sep 81
FY 82	
Additional Format B Hardware Available	Oct 81
1/2 ATR Flow Through Module Available	Mar 82
IR Development Hardware Available	May 82
SE Development Hardware Available	Sep 82

FY 83

IR Development Testing Complete	Oct 82
SE Development Testing Complete	Mar 83

6.6.1.7 Summary

The MAP program provides a vehicle to address the problems of poor reliability, maintainability, and high life cycle cost that the Navy faces with current avionics system. If future acquisitions of new aircraft and the associated avionics systems are to gain the advantages offered by standardization, a concentrated effort must be sustained and supported to allow application in as many systems as possible.

6.6.2 AVIONICS COMPONENTS AND SUBSYSTEMS (AVCS)

6.6.2.1 Background

The Avionics Components and Subsystems (AVCS) program was formulated by NAVAIR to reduce proliferation of unique avionic equipment and reduce life cycle costs by providing a family of Government Furnished Equipment (GFE) common to multiple aircraft types. The AVCS program provides for the development of avionic equipment supportive of, but separate from major weapon system acquisitions. The objectives and goals of the AVCS program are as follows:

* Reduce proliferation of weapon system unique avionics by developing common GFE for application to multiple aircraft.

* Select for development those avionics subsystems that have near term as well as future application.

* Define common GFE subsystems via a NAVAIR performance specification.

* Develop common avionic subsystems which have the potential to achieve high reliability, easy maintainability, logistic supportability and low life cycle cost.

* Maximize commonality of hardware and software across multiple aircraft types at the Weapon Replaceable Assembly (WRA) and Shop Replaceable Assembly (SRA) levels. The SRAs will consist of a core set that may be used in multiple aircraft applications and special SRAs that have limited application for individual aircraft peculiar functions.

* Implement SRA form factors that result in easily replaceable, low-cost, plug-in modules which are non-proprietary, functionally specifiable and testable. Use of form factors developed by the Modular Avionics Packaging (MAP) program is required.

* Select Weapon Replaceable Assembly (WRA) form factor(s) that are compatible with ARINC Specification 600 for enclosure dimensions and applicable to multiple aircraft. The size of the four Modu-

lar Concept Units (MCU) enclosure as defined in ARINC Specification 600 has been identified as the AVCS baseline. Enclosures developed by the MAP program shall be used where appropriate.

* Maximize flexibility and growth potential by careful subsystem architecture, functional partitioning, use of modularity and incorporation of MIL-STD-1553 interface capability, where applicable.

* Select mature technologies, suitable for military avionic applications, that will be available and logistically supportable for the projected service life of the AVCS equipment.

* Minimize the need for organizational level Ground Support Equipment (GSE) by careful system architecture design and functional partitioning, and by implementing Built-In-Test (BIT) and In-Flight Performance Monitoring (IFPM) to meet fault detection and isolation requirements. If GSE is required, general test equipment or preferred GSE from NAVAIR-16-1-525 shall be used.

* Comply with the Navy's standardization policies on processor architecture and software.

* Provide common GFE avionics to Weapon System Managers via competitive contracts to industry. For each AVCS subsystem development, a complete design disclosure data package shall be procured and then validated by the Navy for support of competitive acquisition on a low-risk, configuration controlled basis.

6.6.2.2 Current Status

The core avionic subsystem candidates currently selected for development under the AVCS program are:

* Digital Air Data Computer (DADC)

* Intercommunications System (ICS)

* Extremely High Frequency (EHF) Data Link for Carrier Aircraft Inertial Navigation System (CAINS)

* Flight Incident Recorder (FIR).

These projects are discussed in more detail under their respective core avionics categories within this plan.

Other AVCS candidates are being investigated within the Navy and by participation on the Air Force Standardization Subpanel for Common/Commercial Avionics. Joint service working groups are in existence and active in formulating and refining interservice cooperation on the AVCS sponsored DADC and ICS projects.

6.6.2.3 Perceived Trends

Digital design techniques and MIL-STD-1553 bus-structured architectures will aid the development of common/standard avionics.

Tri-service cooperation in defining requirements and pursuing common/standard avionics developments is increasing and will continue to increase during the 1980's.

A LCC analysis will need to be performed for each candidate to quantify cost savings attainable through AVCS projects.

6.6.2.4 Areas Requiring Further Development

The AVCS Mini-Navy Decision Coordinating Paper (NDCP) and this NAVAIR Avionics Master Plan (NAMP) are the main Navy planning documents which will be used to present specific plans for AVCS avionics developments. AVCS program planning for avionics developments also includes Tri-Service and NATO liaison and coordination. These latter efforts and the selection of AVCS candidates are being accomplished on a continuing basis.

Short Term (0 to 5 years) -

* Formalize the AVCS candidate selection process.

* Prepare AVCS Acquisition Strategies.

* Investigate and establish a Tri-Service avionics life cycle cost (LCC) analysis program.

* Continue and expand the Tri-Service coordination on avionics candidate identification, selection and development.

* Apply the Modular Avionics Packaging (MAP) hardware elements to AVCS developments.

Mid Term (5 to 10 years) -

* Continue the AVCS candidate selection process.

* Continue the Tri-Service avionics coordination and development efforts.

* Provide increased funding levels to accelerate AVCS developments.

Long Term (10 years plus) -

* The AVCS Program is of a continuing nature and new avionics standardization developments will be pursued.

6.6.2.5 Development Priorities

The AVCS candidate development priorities are as follows:

* DADC

* ICS

* EHF Data Link for CAINS

* FDR

6.6.2.6 Summary

The potential savings in acquisition, operations and support costs through the use of standard avionics have been addressed numerous times by the Executive Branch, the Congress, DoD and the Navy. The AVCS Program is an extremely important step in achieving Navy objectives for more effective management, development and cost effective life cycle support of common/ standard avionics.

GLOSSARY

A

AA	-	Avionics Architect
ACLS	-	Aircraft Carrier Landing System
A/D	-	Analog-to-Digital
ADC	-	Air Data Computer
ADI	-	Attitude Director Indicator
ADM	-	Advanced Development Model
ADS	-	Air Data System
AERMIP	-	Aircraft Equipment Reliability and Maintainability Improvement Program
AEW	-	Airborne Early Warning
AF	-	Air Force
AFAL	-	Air Force Avionics Laboratory
AFCS	-	Automatic Flight Control System
AFSC	-	Air Force Systems Command
AHRS	-	Attitude Heading Reference System
AI	-	Attitude Indicator
AIDS	-	Advanced Integrated Display System
AIMD	-	Aircraft Intermediate Maintenance Department
AJ	-	Anti-jam
AM	-	Amplitude Modulation
AM	-	Acquisition Manager
AMEN	-	Aviation Maintenance Engineering Analysis System
AMP	-	Analytical Maintenance Program
AOP	-	Air Operational Program
ARINC	-	Aeronautical Radio, Inc.
ASU	-	Approval for Service Use
ASW	-	Antisubmarine Warfare
AT	-	Automatic Testing
ATE	-	Automatic Test Equipment
ATG	-	Automatic Test Generation
ATO	-	Air Tactical Officer
ATPG	-	Automatic Test Procedure Generation
ATR	-	Austin Trumbell Radio
AVCS	-	Avionics Components and Subsystems

B

BASIC	-	Basic Avionics System Integration Concept
BDHI	-	Bearing, Distance, Heading Indicator
BIT	-	Built In Test
BIU	-	Bus Interface Unit
BORAM	-	Block-Organized RAM

C

C_3^2RDB	-	Command Control Requirements Data Base
C^3	-	Communications, Command, Control
C^3NI	-	Communications, Command, Control, Navigation, Identification
CAD	-	Computer Aided Design
CAINS	-	Carrier Aircraft Inertial Navigation System
CCD	-	Charge Coupled Device
CDS	-	Combat Direction Systems
CDU	-	Control Display Unit
CFA	-	Cognizant Field Activity
CFE	-	Contractor Furnished Equipment
CIA	-	Complex Integrated Assemblies
CILOP	-	Conversion In Lieu of Procurement
CMOS	-	Complementary MOS
CMS-2	-	Compiler Monitor System - 2
CMUX	-	Converter - Multiplexer
CNI	-	Communication, Navigation, Identification
CNO	-	Chief of Naval Operations
COMPRESS	-	COMmercial PRoduction of Electronics Solid-state Systems
COMSEC	-	Communication Security
CPU	-	Central Processor Unit
CRT	-	Cathode Ray Tube
CV	-	Aircraft Carrier
CVS	-	Correlation Velocity Sensor
CW	-	Continuous Wave

D

D/A	-	Digital-to-Analog
DABS	-	Discrete Address Beacon System
DADC	-	Digital Air Data Computer
DAIS	-	Digital Avionics Information System
DASL	-	Digital Avionic Systems Laboratory
DCA	-	Dual-dual Computer Assemblies
DMA	-	Direct Memory Access
DMD	-	Data Management Display
DME	-	Distance Measuring Equipment
DOD, DoD	-	Department of Defense
DRO	-	Destructive Read-Only
DSARC	-	Defense Systems Acquisition Review Council
DTDMA	-	Distributed Time Division Multiple Access
DTL	-	Diode-Transistor Logic
DVS	-	Doppler Velocity Sensor

E

EAPROM	-	Electrically Alterable PROM
EAROM	-	Electrically Alterable ROM
ECCM	-	Electronic Counter-Counter Measures
ECL	-	Emitter Coupled Logic
ECM	-	Electronic Counter Measures
ECP	-	Engineering Change Proposal
EDM	-	Engineering Development Model
EEPROM	-	Electrically Erasable PROM
EHF	-	Extremely High Frequency
EHSI	-	Electronic Horizontal Situation Indicator
EIOP	-	Enhanced Input, Output Processor
EIP	-	Engineering Investigation Program
EL	-	Electroluminescent
ELOS	-	Extended Line-Of-Sight
EMI	-	Electromagnetic Interference
EMP	-	Electromagnetic Pulse
EO	-	Electro-Optical
EPROM	-	Erasable Programmable Read-Only Memory
ESM	-	Electronic Support Measures
EW	-	Electronic Warfare

F

FADEC	-	Full Authority Digital Electronic Controls
FCD	-	Flight Critical Displays
FDM	-	Frequency Division Multiplex
FDR	-	Flight Data Recorder
FDS	-	Flight Director System
FET	-	Field Effect Transistor
FLR	-	Forward Looking Infrared
FM	-	Frequency Modulation
FO	-	Fiber Optics
FOC	-	Full Operational Capability
FOV	-	Field of View
FSD	-	Full Scale Development
FTBA	-	Flight Test Bed Aircraft
FY	-	Fiscal Year

G

GaAs	-	Gallium Arsenide
GCA	-	Ground Controlled Approach
GFE	-	Government Furnished Equipment
GHz	-	Gigahertz (10^9 or 1 billion hertz)
GPS	-	Global Positioning System
GSE	-	Ground Support Equipment

H

HMOS	-	High Performance NMOS
HOL	-	Higher Order Language
HOTAS	-	Hands-On-Throttle and Stick
HMD	-	Helmet Mounted Display
HSD	-	Horizontal Situation Display
HSI	-	Horizontal Situation Indicator
HUD	-	Heads-Up-Display

I

IC	-	Integrated Circuit
ICS	-	Intercommunications System
IEEE	-	Institute of Electrical, Electronic Engineers
IF	-	Intermediate Frequency
IFF	-	Identification Friend or Foe
IFLT	-	Improved Fatigue Life Tracking
IFPM	-	Inflight Performance Monitoring
IISA	-	Integrated Inertial Sensor Assembly
I^2L	-	Integrated-Injection Logic
ILS	-	Integrated Logistics Support
IMPACT	-	Impact of Microcircuit Part Obsolescence on Avionic Critical Technology
IMPATT	-	Impact Avalanche Transit Time
INS	-	Inertial Navigation System
IO	-	Integrated Optics
I/O	-	Input/Output
IOC	-	Initial Operational Capability
IOT&E	-	Initial Operational Test & Evaluation
IR	-	Infrared
IR	-	Integrated Rack
IRC	-	Integrated Radio Controls
ISA	-	Inertial Sensor Assembly
ISEM	-	Improved Standard Electronic Module
ITF	-	Integrated Test Facility

J

JLC	-	Joint Logistics Commanders
JTIDS	-	Joint Tactical Information Distribution System

L

LAMPS	-	Light Airborne Multipurpose System
LED	-	Light Emitting Diode
LC	-	Liquid Crystal
LCC	-	Life Cycle Cost
LCD	-	Liquid Crystal Display
LCSR	-	Limited Continuous Speech Recognition
LLTV	-	Low Light-Level Television
LOS	-	Line-of-Sight
LSI	-	Large Scale Integration

M

MAP	-	Modular Avionics Packaging
MBPS	-	Megabits Per Second
MCD	-	Monitor Control Display
MCU	-	Modular Concept Unit
MEECN	-	Minimum Essential Emergency Communication Network
MFHBF	-	Mean Flight Hours Between Failure
MFHBMA	-	Mean Flight Hours Between Maintenance Action
MFPK	-	Multi Function Programmable Keyboard
MHz	-	Megahertz
MIC	-	Microwave Integrated Circuit
MIL-STD	-	Military Standard
MIMD	-	Multiple Instruction Multiple Data
MLS	-	Microwave Landing System
MMD	-	Mission Management Display
MMR	-	Multimode Receiver
MNOS	-	Metal Nitride Oxide Semiconductor
MOS	-	Metal Oxide Semiconductor
MPD	-	Multi-Purpose Display
MRAALS	-	Marine Remote Area Approach and Landing System
MT	-	Manufacturing Technology
MTASS	-	Machine Transferable Support Software
MTBF	-	Mean Time Between Failure
MTTR	-	Mean Time to Repair
MUX	-	Multiplex

N

NAC	-	Naval Avionics Center
NADC	-	Naval Air Development Center
NAESU	-	NAVAIR Engineering Service Unit
NALDA	-	Naval Aviation Logistics Data Analysis
NAMP	-	NAVAIR Avionics Master Plan
NAMSO	-	Navy Maintenance Support Office
NASA	-	National Aeronautic and Space Agency
NATO	-	North Atlantic Treaty Organization
NAVAIR	-	Naval Air Systems Command

N (Cont'd)

NAVSEA	-	Naval Sea Systems Command
NAVSTAR	-	Navigation Satellite Timing and Ranging
NDCP	-	Navy Decision Coordinating Paper
NDRO	-	Non-Destructive Read-Only
NESO	-	NAVAIR Engineering Support Office
NFSR	-	NAVAIR Field Service Representatives
NMC	-	Naval Material Command
NMOS	-	N-Channel Metal Oxide Semiconductor
NPE	-	Navy Preliminary Evaluation
NSA	-	National Security Agency
NSIU	-	Navigation Switching Interface Unit
NTDS	-	Navy Tactical Data System
NTE	-	Naval Technical Evaluation
NTEC	-	Naval Training Equipment Center
NUSC	-	Naval Underwater Systems Center

O

O&M,N	-	Operations & Maintenance, Navy
OFS	-	Operational Flight Software
ONT	-	Office of Naval Technology
OPEVAL	-	Operational Evaluation
OPNAV	-	Office of Chief of Naval Operations
OSIP	-	Operational Safety & Improvement Program

P

PAR	-	Predict and Relook
PASU	-	Preliminary Approval for Service Use
PCSB	-	Pulse Coded Scanning Beam
PDL	-	Program Design Language
PFA	-	Participating Field Activity
PGSE	-	Peculiar Ground Support Equipment
POM	-	Program Objective Memorandum
PRAM	-	Productivity, Reliability, Availability & Maintainability
PSK	-	Phase Shift Keying

R

R&M	-	Reliability & Maintainability
R&D	-	Research and Development
RDT&E	-	Research, Development, Test & Evaluation
RAM	-	Random-Access Memory
RCS	-	Required Course Synchro
RF	-	Radio Frequency
RFP	-	Request for Proposal
RISE	-	Readiness Improvement Status Evaluation
RLG	-	Ring Laser Gyro
RMI	-	Radio Magnetic Indicator

R (Cont'd)

RMS	-	Root Mean Square
RNS	-	Radar Navigation Set
ROM	-	Read-Only Memory
RPV	-	Remotely Piloted Vehicle
RTL	-	Resistor-Transistor Logic

S

SAE	-	Society of Automotive Engineers
SAL	-	Standard Assembly Language
SAM	-	Standard Avionics Module
SAR	-	Synthetic Aperture Radar
SAW	-	Surface Acoustic Wave
SDC	-	Signal Data Converter
SDDL	-	Software Design and Doumentation Language
SE	-	Standard Enclosure
SEM	-	Standard Electronic Module
SIMD	-	Single Instruction Multiple Data
SINCGARS	-	Single Channel Ground Air Radio System
SIT	-	Static Induction Transistor
SLEP	-	Service Life Extension Program
SO	-	Sensor Operator
SOCMOS	-	Silicon Gate CMOS
SOS	-	Silicon-On-Sapphire
SRA	-	Shop Replacable Assembly
SREM	-	Software Requirments Engineering Methodology
SSA	-	Software Support Activity

T

TACAN	-	Tactical Air Navigation
TDMA	-	Time Division Multiple Access
TECHEVAL	-	Technical Evaluation
TFEL	-	Thin-Film Electroluminescent
TIES	-	Tactical Information Exchange System
TOA	-	Time of Arrival
TRAPATT	-	Trapped Plasma Avalanche Triggered Transit
TTL, T^2L	-	Transistor-Transistor Logic
TWT	-	Traveling Wave Tube

U

UFC	-	Up Front Control
UHF	-	Ultra High Frequency
UVEPROM	-	Ultraviolet EPROM
UVPROM	-	Ultraviolet PROM

V

VAST	-	Versatile Avionics System Tester
VHSIC	-	Very High Speed Integrated Circuits
VHF	-	Very High Frequency
VIS	-	Voice Interactive System
VLSI	-	Very Large Scale Integration
VRAS	-	Voice Recognition and Synthesis
VSD	-	Vertical Situation Display
VSTOL	-	Vertical, Short Take-Off & Landing

W

WRA	-	Weapons Replaceable Assembly
WSAA	-	Weapons Systems Support Activity


DATE
ILME